Are we headed for a complexity apocalypse for embedded SoCs
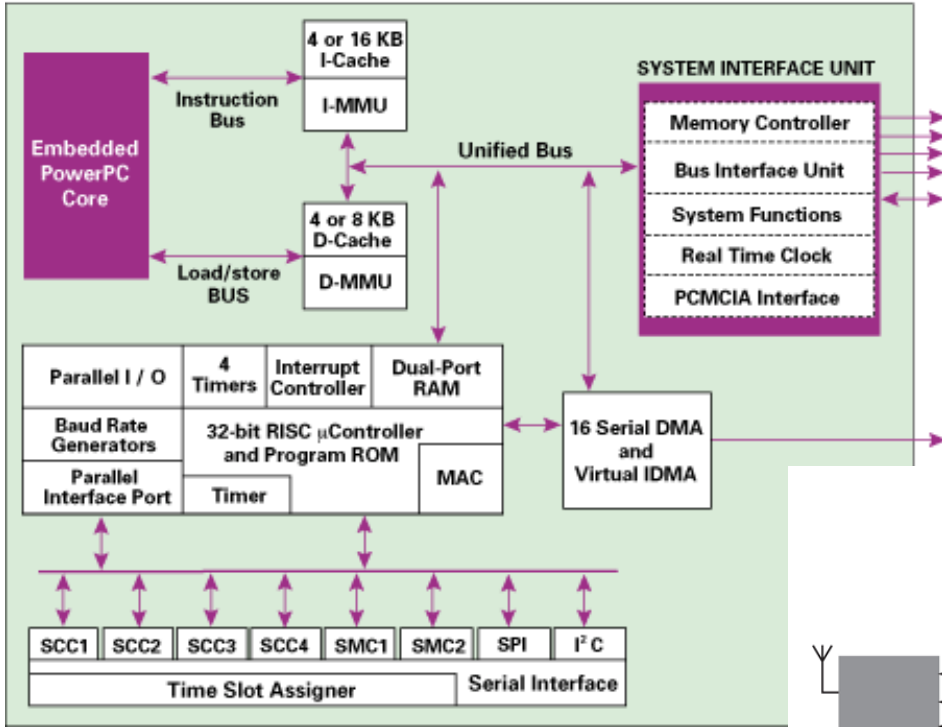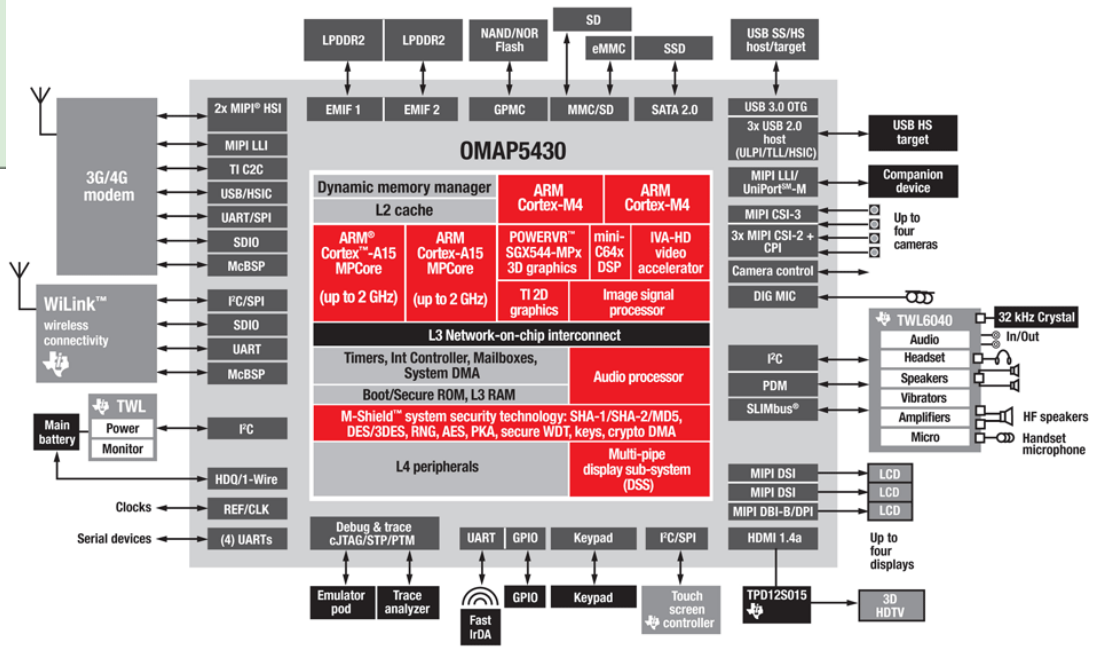
Matthew Locke
Director, Linux Development Center
Texas Instruments
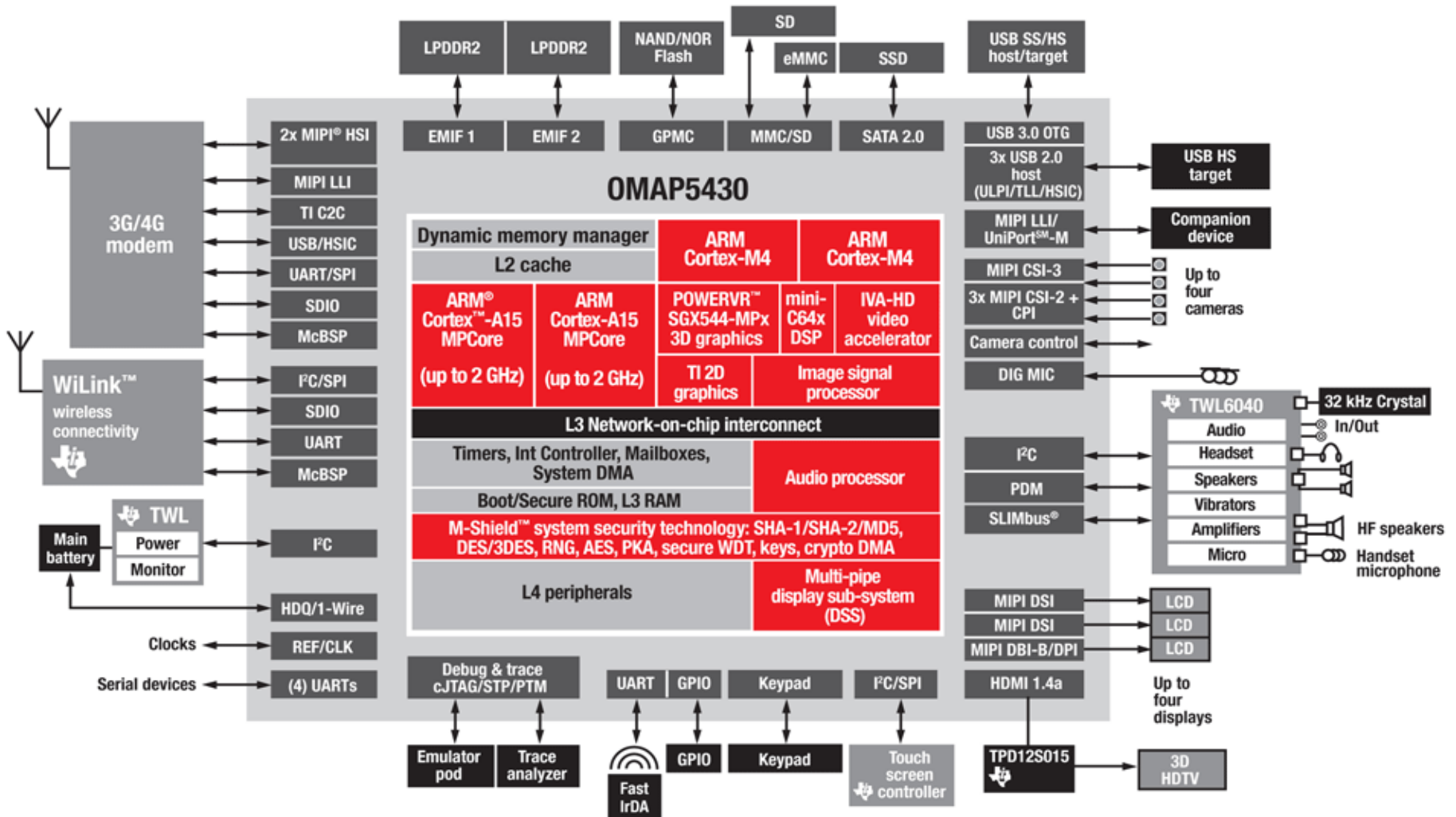
TEXAS INSTRUMENTS

MPC860 Block Diagram

Embedded PowerPC Core

Instruction Bus

4 or 16 KB I-Cache

I-MMU

Unified Bus

SYSTEM INTERFACE UNIT

- Memory Controller
- Bus Interface Unit
- System Functions
- Real Time Clock
- PCMCIA Interface

4 or 8 KB D-Cache

D-MMU

Load/store BUS

Parallel I / O | 4 Timers | Interrupt Controller | Dual-Port RAM

Baud Rate Generators

32-bit RISC μController and Program ROM

Parallel Interface Port | Timer | MAC

16 Serial DMA and Virtual IDMA

SCC1 | SCC2 | SCC3 | SCC4 | SMC1 | SMC2 | SPI | I²C

Time Slot Assigner | Serial Interface

TEXAS INSTRUMENTS
OMAP

TI OMAP5430 SoC

LPDDR2 | LPDDR2 | NAND/NOR Flash | SD | | USB SS/HS host/target
| | | eMMC | SSD |

2x MIPI HSI | EMIF 1 | EMIF 2 | GPMC | MMC/SD | SATA 2.0 | USB 3.0 OTG
MIPI LLI | | | | | | 3x USB 2.0 host (ULPI/TLL/HSIC)
TI C2C | | | | | | USB HS target
USB/HSIC | **OMAP5430** | | | | | MIPI LLI/ UniPort℠-M
UART/SPI | | | | | | Companion device
SDIO | Dynamic memory manager | ARM Cortex-M4 | ARM Cortex-M4 | MIPI CSI-3
McBSP | L2 cache | | | 3x MIPI CSI-2 + CPI

3G/4G modem

ARM Cortex™-A15 MPCore (up to 2 GHz) | ARM Cortex-A15 MPCore (up to 2 GHz) | POWERVR™ SGX544-MPx 3D graphics | mini-C64x DSP | IVA-HD video accelerator

| | | TI 2D graphics | Image signal processor | Camera control

Up to four cameras

WiLink™ wireless connectivity

I²C/SPI | L3 Network-on-chip interconnect | DIG MIC
SDIO | Timers, Int Controller, Mailboxes, System DMA | Audio processor
UART | Boot/Secure ROM, L3 RAM |
McBSP | M-Shield™ system security technology: SHA-1/SHA-2/MD5, DES/3DES, RNG, AES, PKA, secure WDT, keys, crypto DMA

L4 peripherals | Multi-pipe display sub-system (DSS)

32 kHz Crystal
In/Out

TWL6040
Audio | Headset
Speakers
Vibrators
Amplifiers | HF speakers
Micro | Handset microphone

I²C
PDM
SLIMbus®

TWL Power | Monitor
Main battery

I²C

HDQ/1-Wire

REF/CLK | Clocks

(4) UARTs | Serial devices

MIPI DSI | LCD
MIPI DSI | LCD
MIPI DBI-B/DPI | LCD

Up to four displays

Debug & trace cJTAG/STP/PTM | UART | GPIO | Keypad | I²C/SPI | HDMI 1.4a | TPD12S015 | 3D HDTV

Emulator pod | Trace analyzer | GPIO | Keypad | Touch screen controller

Fast IrDA

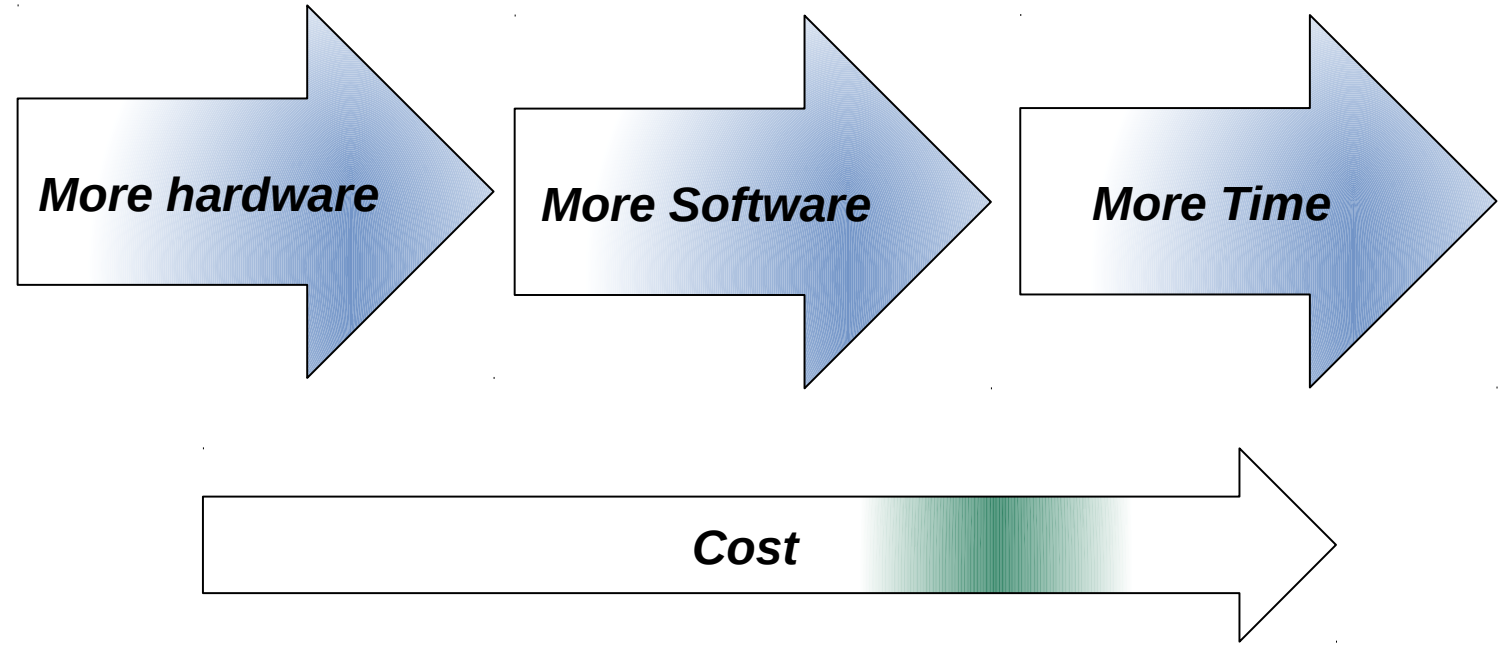
TEXAS INSTRUMENTS

TI OMAP5430 SoC

Complexity Factors

Squeeze more in

Physical limitations – size, power, thermal

Focused Differentiation

Compute requirements

Complexity variables

More hardware → **More Software** → **More Time**

Cost →

Time to Market pressure is not shrinking

The Software Problem

−Does everything go upstream?

−Do some features become "product" only?

−How does the kernel evolve to handle this complexity?

−Can it evolve fast enough?

−Who is doing all this work?

What's the solution?

Change how we think and work
- Software starts earlier
- Hardware and software relationship
- Software led decisions

What's the solution?

Shared Engineering

– Linux Foundation

– Linaro

– Open Engineering?

What's the solution?

Yes, must continue to upstream

Minor Apocalypse

Minor Apocalypse results

- Device Tree
- Dmaengine
- pinctl
- Common clock framework
- rpmsg

What's next