The Project: An Open Platform

• SuperH Compatible Open Chip Platform & DSPs
  – Why these choices, and why now?

• Open Chip Designs, Open Hardware
• Open Software Platform
• Community

• Silicon, Hardware, Signal Processing, OS & Software
  – IoT Platform
Community Design & License

- OPF Certifies FPGA and ASIC. Validation Vectors.
- Professional Support from Multiple Service Providers Distributed Globally
- Liberal License Terms: BSD and Community HW License

OpenSource
J Core CPU
S Core DSP
Architecture
And RTL

Community
www.OPF.org
www.NoMMU.org
Devices

Linux
uClinux
Android

Hardware
Service
Providers

Software
Service
Providers

Community Hardware License / BSD

GNU Public License / BSD

Downloads

Contributions

Design Support
Community Design & License

- OPF Certifies FPGA and ASIC. Validation Vectors.
- Professional Support from Multiple Service Providers Distributed Globally
- Liberal License Terms: BSD and Community HW License

OpenSource
J Core CPU
S Core DSP
Architecture
And RTL

Linux
uClinux
Android

Community Hardware License / BSD

GNU Public License / BSD

Downloads

Contributions

VHDL Code Drop
Mid 2015
Use on a simple FPGA Board

Hardware Service Providers

Software Service Providers

Design Support

Design Support

www.OPF.org
www.NoMMU.org
Community Design & License

- OPF Certifies FPGA and ASIC. Validation Vectors.
- Professional Support from Multiple Service Providers Distributed Globally
- Liberal License Terms: BSD and Community HW License

Open Source J Core CPU S Core DSP Architecture And RTL

Community Hardware License / BSD

Downloads

Community
www.OPF.org www.NoMMU.org

Devices

Downloads

Linux uClinux Android

Complete Linux Stack (Connectivity)

Contributions

Design Support

Software Service Providers

Hardware Service Providers

Use on a simple FPGA Board

VHDL Code Drop Mid 2015
J Series Computation Core Cluster Roadmap

Unit: Arithmetic Operations per Second

- **2014**:
  - **J2**: 32b RISC
    - Generic IoT Devices

- **2015**: 2016
  - **J2+**: 32b RISC SMP + S-Core DSP Array
    - Signal Processing IoT
    - Next Generation Power
    - Transmission and Distribution,
      Medical,
      Infrastructure,
      Sensors

- **2017**: 2017
  - **J4**: 32b RISC SMP + SIMD Array
    - Driver Assist Subsystems in Automotive

Calendar Year

- **2014**
- **2015**
- **2016**
- **2017**
J Series Computation Core Cluster Roadmap
Unit: Arithmetic Operations per Second

- **J2**: 32b RISC
- **J2+**: 32b RISC SMP + S-Core DSP Array
- **J4**: 32b RISC SMP + SIMD Array

- **2014**: Generic IoT Devices
  - First Device: Smart Energy Instruments
  - IoT / Energy Management SoC FPGA and ASIC implementations
- **2015**: Signal Processing IoT
  - Next Generation Power Transmission and Distribution, Medical, Infrastructure Sensors
- **2016**: Driver Assist Subsystems in Automotive
- **2017**: First Device: Next Generation Power Transmission and Distribution, Medical, Infrastructure Sensors

Calendar Year
Multiprocessor data coherency

D-cache hardware-based snooping
18/36b S-Core DSP

- Development in Progress (Target Completion: June 2015)
J / S Core On-Chip Computational Clusters

- J2 : RISC  (Prototype SoC in FPGA, Customer Projects)
- J2+ : RISC SMP + DSP Array (Product SoC in Progress, 152nm silicon process)
- J4  : RISC SMP + N-Dimensional SIMD Array (Under Planning)
J / S Core On-Chip Computational Clusters

- J2 : RISC (Prototype SoC in FPGA, Customer Projects)
- J2+: RISC SMP + DSP Array (Product SoC in Progress, 152nm silicon process)
- J4 : RISC SMP + N-Dimensional SIMD Array (Under Planning)

IoT devices are all about multiple Real World Signals...
Signals, Silicon, Software ... and Network
Hardware Development Environment

• Simulation & Synthesis
  – GHDL (open VHDL sim)
  – Xilinx ISE (Spartan FPGA)
  – Cadence ASIC toolflow
  – JTAG w/GDB proxy

• FPGA
  – Low Cost Dev Boards
  – System on Module
    • Multiple Vendors
  – Open FPGA Board design
    • (mid 2015)

• ASIC
  – Silicon Proven (2015)
  – Cadence flow, TSMC
  – Low Die Area
    • J2 0.45mm^2 in 0.152nm
RTL Sim->FPGA->ASIC Tool Flow

- ISP in .ods
  - CPU Generator
  - RTL Code
  - SoC Generator
    - SoC Spec .ods
    - C Headers
    - Linux OS Dev Tree
    - Tool Chains
  - Docs
  - Firmware Flow

- Processor Docs
  - Preprocess
  - Wrapper RTL
  - Synth RTL
    - FPGA Synth
    - GHDL RTL Simulator
    - Std Cell Synthesis

- ASIC Flow: Docs
- FPGA: Verification
RTL IP

• Patents:
  – All SH2 patents expired in October, 2014 (RIP)
  – SH4 patents expiring in 2016

• Copyrights:
  – New Canadian Engineers wrote initial RTL.
  – Then Original Hitachi Engineers Validated

• Trade Secret:
  – The Biggest Secret is there is no Secret.

• Contracts:
  – Don’t Apply

• Trademarks
  – This is not an SH, but J series is instruction set compatible
First Real World Device!

J2+ SoC with 16DSPs and Energy Hardware Measurement Accelerators
First Real World Device!

J2+ SoC with 16DSPs and Energy Hardware Measurement Accelerators
Application: A Measurement & Communications Core Platform for Power Grid Devices

Timing – Measurement – Computation – Communication – Control
Software

What Does Software Stack Look Like?
Standard Linux Environment

• Toolchains
  – GCC
  – BinUtils
  – ELF2FLT
  – GDB

• Kernel
  – CPU Specific Patches
  – Board Support
    • Memory, Interrupt Ctrl
    • Drivers (Serial, Eth, SD)

• Userspace
  – uClibc (Moving to MUSL)
  – Toybox + uClinux Dist
  – Initramfs (SD for Config)
Demo
J2 / S2 Evaluation Boards

- FPGA Development System
  - VHDL on ISE® Design Suite
  - Xilinx AES-S6MB-LX6-G Spartan FPGA LX9 Micro Board (LX25)
  - 62.5MHz

- CPU (~45K Gates per Core)
  - 5 Stage RISC pipeline
  - Full Harvard (separate I and D)
  - 2 Processor SMP Configuration

- DSP Array
  - 4 Operation SIMD DSP
  - P / X / Y Memories
  - e.g. 16 DSPs on a Single SoC

- Memory Subsystem
  - 16b LPDDR @200MHz: PLL off mode, low EMI
  - On Chip Boot ROM
  - 0 wait state scratch pad SRAM (64KB)

- Full chip RTL / C co-simulation
  - JTAG Co-simulation and Debug

- Off-Chip Local Bus Access
  - 8B/10B High Speed Serial LVDS Bus
  - 4 pins : 12.5 or 25MByte/sec
  - Interrupts and exceptions also on the same bus
  - Framed protocol, simple (with example)
  - Purpose: Allow test chip to be used w/FPGA
  - Prototyping with FPGA of full speed peripherals
  - Highly flexible, low technical barrier for RTL design
  - Both bus master and slave

OPF Internal Material
New Resource Sites (mid 2015)

• www.NoMMU.org
  – Development HOWTO
    • Platform information
      – Cortex-M, Armv7-j, J2, coldfire, blackfin...
    • Application development
      – Fixed stack, fork vs vfork, elf vs binflat/fdpic, memory fragmentation,
      – Toolchains and test environments
    • System development
      – Existing Linux root filesystem packages
      – QEMU coldfire emulation test platform for package dev
  – Education
    – Tutorials, mailing list
  – Upstream staging
    • Kernel, llvm, musl
    • Buildroot, openembedded
New Resource Sites  (mid 2015)

- **www.0pf.org**
  - VHDL
    - Git repository with full history, under BSD license
    - J2 processor, S1 DSP, SOC with peripherals, makefiles
  - Bitstreams
    - Release binaries built from VHDL for lx9, lx25, and lx45
      - Lx9 entry level FPGA board, <$100 but only space for basic J2
      - Lx25 midrange, space for icache/dcache and ethernet
      - Lx45 space for multiple DSPs
  - Documentation
    - Toolchain install, VHDL howto, community mailing list