OSSNA 2022 RISC-V BoF

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Where We’ve Been
16 Specs Ratified
  ○ 44 Extensions Total
46 Working Groups
  ○ 10 Committees
  ○ 17 SIGs
  ○ 19 Task Groups

2021
2022

- **4 Specs Ratified**
  - Efficient Trace (E-Trace)
  - Supervisor Binary Interface (SBI)
  - UEFI Protocol
  - Multiply without Divide (Zmmul)

- **New Working Groups**
  - Floating Point SIG
  - Vector SIG
  - Control Flow Integrity (CFI) TG
  - Universal Discovery TG
  - ...
What Comes Next?
The Road Ahead

- Profiles
- Platforms
- SEE
- Unified Discovery
- Debug
- Advanced Interrupts
- Packed SIMD
- Total Store Ordering
- Counters (Zicntr, Zihpm)
- Code Size Reduction
- Vector Half Width (Zvfh)
- Bfloat16
- Crypto Vector
- Fast Interrupts
- IOMMU
- IOPMP
How Do We Get There?
Simplified Specification Lifecycle

- Plan
  - Specification Development
    - V0.1 - V0.99
    - Freeze V1.0-rc1
  - Ratification Requirements
    - 45 Day Public Review
  - Spec Complete V1.0
    - TSC & Board Ratification
    - Ratification Ready V1.0
What About Software?
Rich RISC-V Ecosystem
Available Today

HPC
Consumer

Data Center
IoT

Networking

Applications

Infrastructure

Runtimes

Operating Systems

Hypervisor

Boot

Reliable, Serviceable, Diagnosable

Performant

Secure

Debuggable

Services

Trainig

Academia

Research

CI/Testing

Perf Tools

Simulators

Compilers

SAIL

Golden Model

Architectural Tests

OpenSBI

RTL

DV

Implementation Design & Microarchitecture

Silicon

Soft IP
Software Stack Examples Available Today

Storage
- DB
  - ceph
  - nvme-OF

Networking
- Switch
  - OvS
- Load Balancer
  - NGinx

Virtualization
- Guest OS
  - Linux
- OpenSBI
- KVM
- Ovisor

Security
- SSH
- TLS
- OpenSSL

Web Apps
- Stream & Blog
  - WordPress
  - MediaWiki
- Search
  - Apache Solr
  - OpenJDK
- In-Memory
  - redis

In-Memory
- SPDK
  - DPDK

Linux
- Debian
- Ubuntu
- Fedora
- openSUSE

Compile/Build/Run
- BuildRoot
  - Yocto
  - GCC
  - LVM
  - RENODE
  - QEMU

Firmware/BIOS
- OpenSBI

RISC-V
RISC-V Technical Community

- RISC-V Wiki
  https://wiki.riscv.org
- GitHub
  https://github.com/riscv
- Member Mailing Lists
  https://lists.riscv.org
- Public Mailing Lists
  Google Groups
  ISA-DEV, HW-DEV, SW-DEV