Barracuda Internet Radio Module (RIRM2)

Application Note #1

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Introduction

This document provides information on the physical and electrical characteristics of the Barracuda Module. It is intended to assist engineers developing applications based on the Reciva Barracuda Module.

Reference should also be made to the chip manufacturer datasheets.

Block Diagram

A block diagram of the Barracuda Module is shown below.

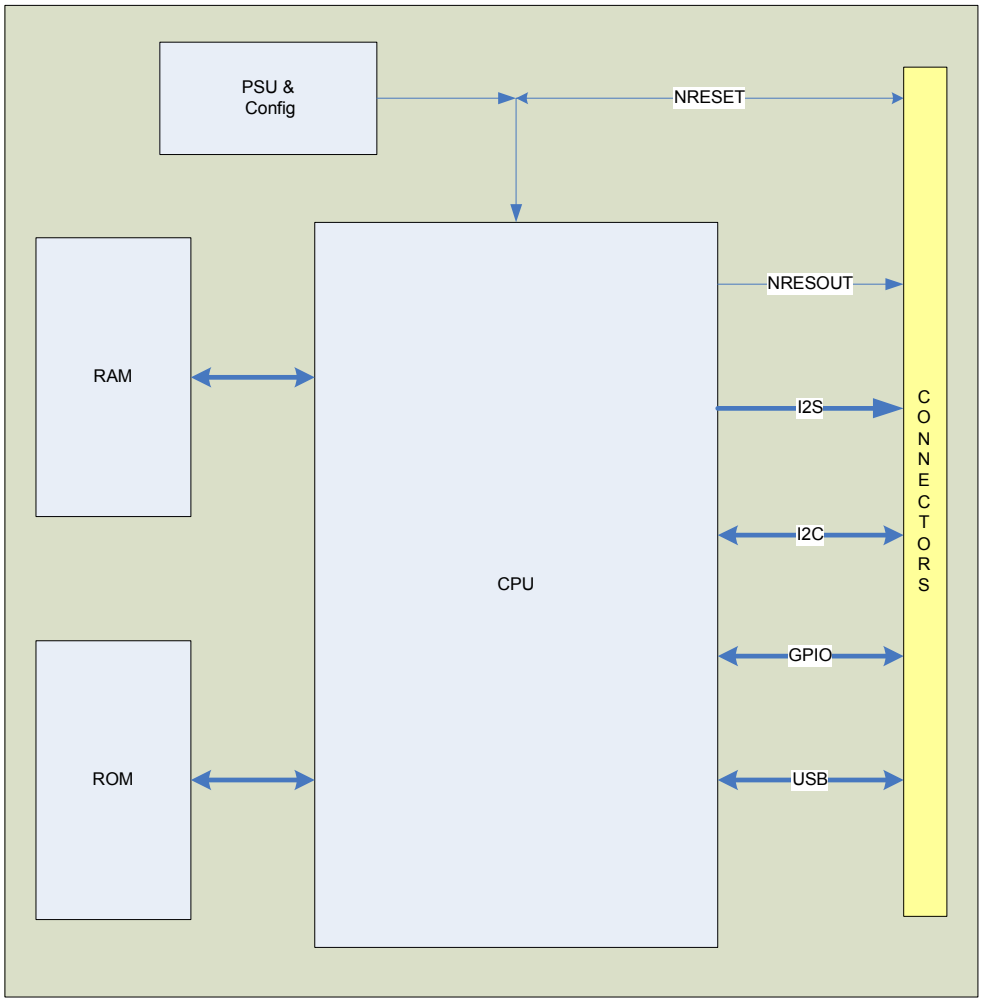

Figure 1 Barracuda Module Block Diagram

Main Components

CPU: S3C2410A-20 from Samsung

Flash: K9F2808U0C-PCB0 from Samsung

RAM: K4S561632E-TC75 from Samsung

IO Connections

The Barracuda Module has three connectors:

J1 & J3 are 20 way (2x10) 2mm pitch pin headers

J2 is a 40 way (2x20) 2mm pitch pin header

Examples of the connectors used are

J1 & J3 Harwin M22-2021005

J2 Harwin M22-2022005

Conn	Pin(s)	Module Signal Name	In/Out	Description/Function	CPU Pin	Notes
J1	2, 11, 14	GND	Power	System Ground		
J1	1, 17	VDD3V3	Power	Logic Supply		
J1	3	SDATA3	IO t8	GPIO SD Card Data	GPE10	
J1	4	CDCLK	IO t8	GPIO DAC Clock	GPE2	
J1	5	SDATA2	IO t8	GPIO SD Card Data	GPE9	
J1	6	I2SSDO	IO t8	GPIO IIS Data Out	GPE4	
J1	7	SDATA1	IO t8	GPIO SD Card Data	GPE8	
J1	8	I2SSCLK	IO t8	GPIO IIS Bit Clock	GPE1	
J1	9	SDATA0	IO t8	GPIO SD Card Data	GPE7	
J1	10	I2SLRCK	IO t8	GPIO IIS Left/Right Clock	GPE0	
J1	12	I2SSDI	IO t8	GPIO IIS Data In	GPE3	
J1	13	SDCMD	IO t8	GPIO SD Card Control	GPE6	
J1	15	SDCLK	IO t8	GPIO SD Card Clock	GPE5	
J1	16	L3CLOCK	IO t8	GPIO Timer 0 Out	GPB0	
J1	18	L3MODE	IO t8	GPIO	GPB7	
J1	19	SCL	IO d8	GPIO I2C Bus Clock	GPE14	
J1	20	L3DATA	IO t8	GPIO	GPB9	

Table 1 Connector J1

Conn	Pin(s)	Signal	In/Out	Description/Function	CPU Pin	Notes
J2	9, 22, 31, 28, 16, 23, 40	GND	Power	System Ground		
J2	2, 4	VSIN	Power	Input to 1.8V Regulator for CPU core		
J2	14, 34	VDD3V3	Power	Logic Supply		
J2	36	VDD1V8	Power	Core 1.8V Output from Regulator		5
J2	38	VDDRTC	Power	1.8V in to RTC block		5
J2	1	NSS1	IO t8	GPIO SPI select 1	GPG3	
J2	3	SPIMISO1	IO t8	GPIO SPI Master In	GPG5	
J2	5	SPIMOSI1	IO t8	GPIO SPI Master Out	GPG6	
J2	6	NC	-	NC	-	1
J2	7	SPICLK1	IO t8	GPIO SPI Clock	GPG7	
J2	8	SDA	IO d8	GPIO I2C Bus Data	GPE15	
J2	10	SDNWP	IO t8	GPIO	GPF1	
J2	11	KBDROW3	IO t12	GPIO	GPG11	
J2	12	SDNCD	IO t8	GPIO	GPF2	
J2	13	KBDROW2	IO t6	GPIO	GPG10	
J2	15	KBDROW1	IO t6	GPIO	GPG9	
J2	17	KBDROW0	IO t6/t8	GPIO	GPG8, GPF0	2
J2	18	USBDP	us	USB Host/Dev Pos	DP1	
J2	19	SHAFT0	IO t12	GPIO	GPG14	
J2	20	USBDN	Us	USB Host/Dev Neg	DN1	
J2	21	SHAFT1	IO t12	GPIO	GPG15	
J2	24	USBHN	us	USB Host Neg	DP0	
J2	25	GIOAN0	IO t8/r10	GPIO Analogue In	GPF4	
J2	26	USBHP	us	USB Host Pos	DP0	
J2	27	GIOAN1	IO t8/r10	GPIO Analogue In	GPF5	
J2	29	GIOAN2	IO t8/r10	GPIO Analogue In	GPF6	
J2	30	NUDEVFSPEED	IO t12	GPIO	GPH10	
J2	32	NUHPWR	IO t12	GPIO	GPH9	
J2	33	NLED_ON	IO t8	GPIO	GPH7	
J2	35	NRESET	IO ts	Reset In Out active low	NRESET	3
J2	37	NRSTOUT	O b8	Reset Out Active low	NRSTOUT	
J2	39	PWREN	O b8	Core Power Control	PWREN	

Table 2 Connector J2

Conn	Pin(s)	Signal	In/Out	Description/Function	CPU Pin	Notes
J3	1, 8, 19	GND	Power	System Ground		
J3	2	KBDCOL2	IO t8	GPIO	GPD10	
J3	3	LCDD7	IO t8	GPIO VDAT	GPC15	
J3	4	KBDCOL1	IO t8	GPIO	GPD9	
J3	5	LCDD6	IO t8	GPIO VDAT	GPC14	
J3	6	KBDCOL0	IO t8	GPIO	GPD8	
J3	7	LCDD5	IO t8	GPIO VDAT	GPC13	
J3	9	LCDD4	IO t8	GPIO VDAT	GPC12	
J3	10	LCDCN5	IO t8	GPIO VCNT	GPC5	
J3	11	LCDD3	IO t8	GPIO VDAT	GPC11	
J3	12	LCDCN4	IO t8	GPIO, TOUT & VCNT	GPC4, GPB1	2
J3	13	LCDD2	IO t8	GPIO VDAT	GPC10	
J3	14	LCDCN3	IO t8	GPIO VCNT	GPC3	
J3	15	LCDD1	IO t8	GPIO VDAT	GPC9	
J3	16	LCDCN2	IO t8	GPIO VCNT	GPC2	
J3	17	LCDD0	IO t8	GPIO VDAT	GPC8	
J3	18	LCDCN1	IO t8/ot	GPIO, TOUT & CS2	GPC1, GPB3, GPA13	4
J3	20	LCDCN0	IO t8/ot	GPIO, TOUT & CS1	GPC0, GPB2, GPA12	4

Table 3 Connector J3

Descriptions of the IO Types

IO Type	Description	Notes
us	USB pad	
ot	Output pad, tri-state, Io = 8mA	
b8	Output pad, Io = 8mA	
r10	Analog input	
t6	Bi-directional 5V tolerant LVCMOS schmitt-trigger, 100Kohm pull-up resistor with control, tri-state, Io = 6mA	
t8	Bi-directional LVCMOS schmitt-trigger, 100Kohm pull-up resistor with control, tri-state, Io = 8mA	
t12	Bi-directional LVCMOS schmitt-trigger, 100Kohm pull-up resistor with control, tri-state, Io = 12mA	
d8	Bi-directional LVCMOS schmitt-trigger, 100Kohm pull-up resistor with control, open-drain, Io = 8mA	
ts	Bi-directional 50Kohm pull-up resistor with control, tri-state, Io = 8mA	

Table 4 IO Types

Notes

1. Not Connected
2. Two (or more) IOs connected to this pin. Maximum one output driven at any time
3. J2-35 NRESET is a tri-state IO with pull-up. Only to be driven through a resistor >1k Ohms. During the power up this signal is driven by the power-on reset chip (ATtiny12).
4. Two IOs plus a chip select. Maximum one output driven at any time
5. J2 pin 38 needs to be supplied with 1.8V. To do so J2 pin 36 can be connected to it.

Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Range	Unit	Notes
DC Supply	VDD3V3	0 to +3.6	V	
DC Supply Reg in	VSIN	0 to +5.5	V	
DC Input voltage	VIN	GND-0.2 to VDD3V3+0.2	V	
Storage Temperature	TSTG	-10 to 80	Deg C	

Table 5 Absolute Maximum Ratings

Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
DC Supply	VDD3V3	3.15		3.45	V	
DC Supply Regulator in	VSIN	3.15		3.45	V	
DC Input High	VIH	2.0			V	
DC Switching threshold	VT		1.4		V	
DC Input Low	VIL			0.8	V	
DC Output High	VOH	2.4			V	
DC Output Low	VOL			0.4	V	
Core Current	I(VSIN)		140	180	mA	A
Logic Current	I(VDD3V3)		40	70	mA	A
DC Supply rise time	RT			60	Ms	
DC Supply Below trigger time	BTT	7			Us	
DC Supply Trigger Rising	VTR	1.0	1.4	1.8	V	
DC Supply Trigger Falling	VTF	0.4	0.6	0.8	V	
Operating Temperature	TOP	0		55	Deg C	

Table 6 Recommended Operating Conditions

Notes

A. Power consumption is dependent on software activity.

DC Supply Characteristics

This diagram shows the limits of the power supply that the PSU must obey to ensure that the module functions correctly. For example if the power supply voltage goes underneath DC supply min, it has also to go underneath VTR and VRF for a certain period of time BTT before going back to normal.

The power supply voltages (VDD3V3 and VSIN) have to be applied simultaneously and have to be stable within RT (60ms).

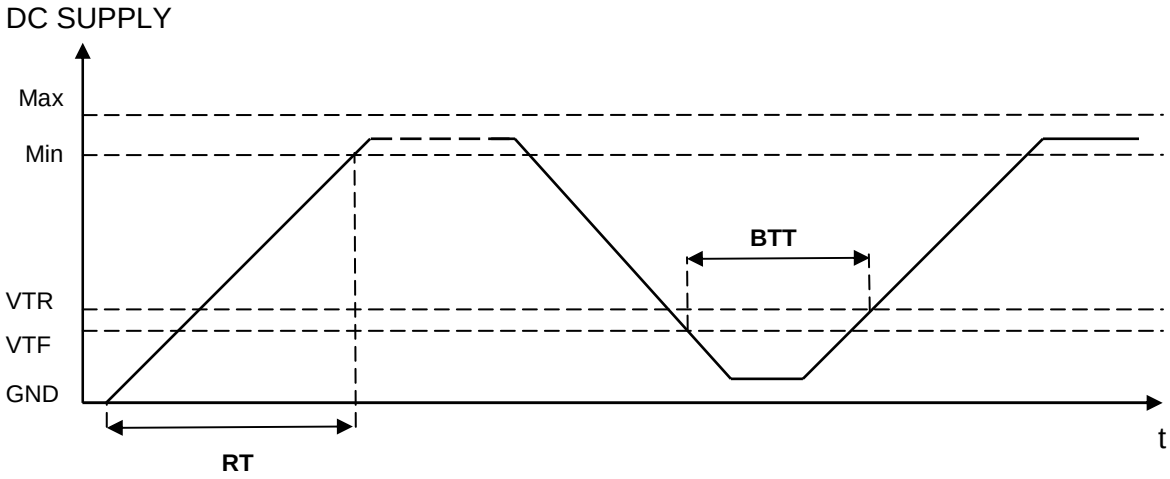

Figure 2 Supply Characteristics

Test Points Arrangement

Test Point Location (back view)

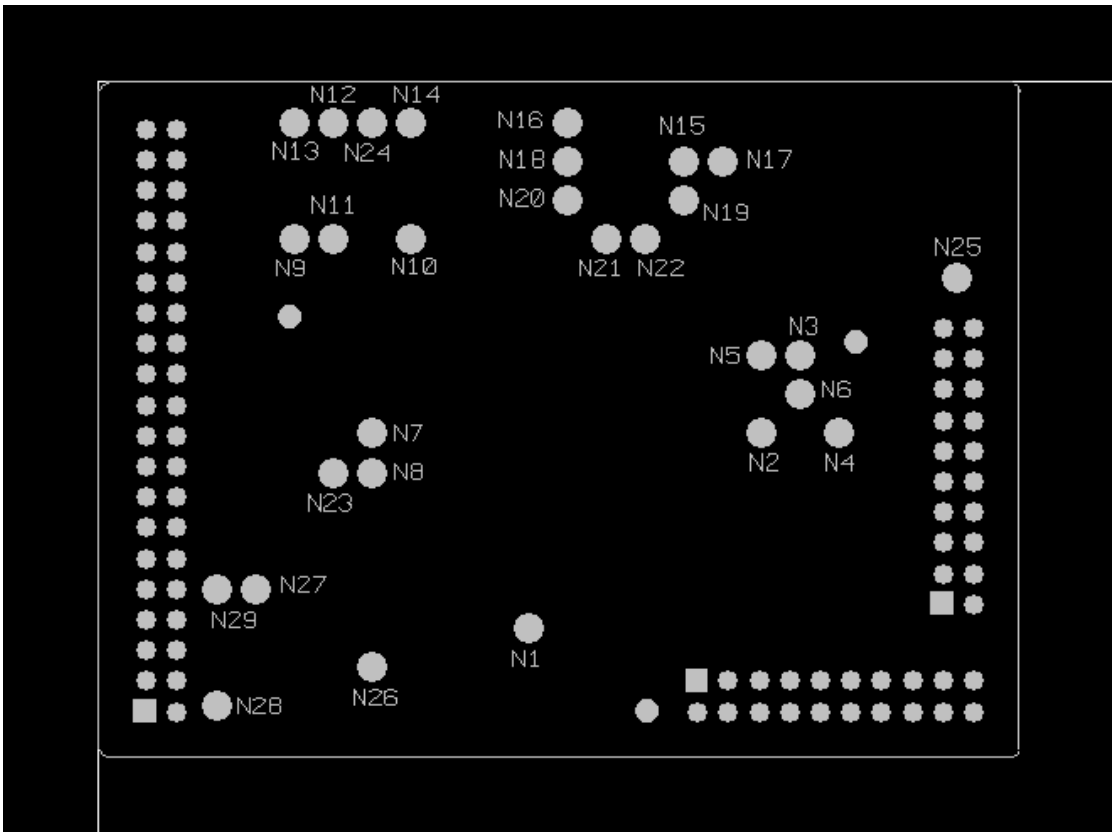

Figure 3 Test Point Location

Test Point Description

Pad	Signal	Description	Note
N2	TMS	JTAG (10K pull-up on-board)	
N3	TDO	JTAG	
N4	TDI	JTAG	
N5	TCK	JTAG	
N6	nTRST	JTAG (10K pull-up on-board)	
N9	FRnB	Flash	
N10	nFRE	Flash (Pad connected to flash pin. 220R fitted between CPU and Flash	
N11	nFRC	Flash (Pad connected to flash pin. 220R fitted between CPU and Flash	
N12	nWP	Flash (Pad connected to flash pin. 220R fitted between CPU and Flash	
N13	nCLE	Flash (Pad connected to flash pin. 220R fitted between CPU and Flash	
N14	nALE	Flash (Pad connected to flash pin. 220R fitted between CPU and Flash	
N15	D0	Flash	
N16	D1	Flash	
N17	D2	Flash	
N18	D3	Flash	
N19	D4	Flash	
N20	D5	Flash	
N21	D6	Flash	
N22	D7	Flash	
N24	nFWE	Flash (Pad connected to flash pin. 220R fitted between CPU and Flash	
N25	GND	Power	
N26	VDD1V8	Power	
N27	VDD3V3	Power	
N28	VSIN	Power	
N29	GND	Power	

Table 7 Test Points

Mechanical Data

The electronic components on the Barracuda Module are mounted on the same side as the IO connectors

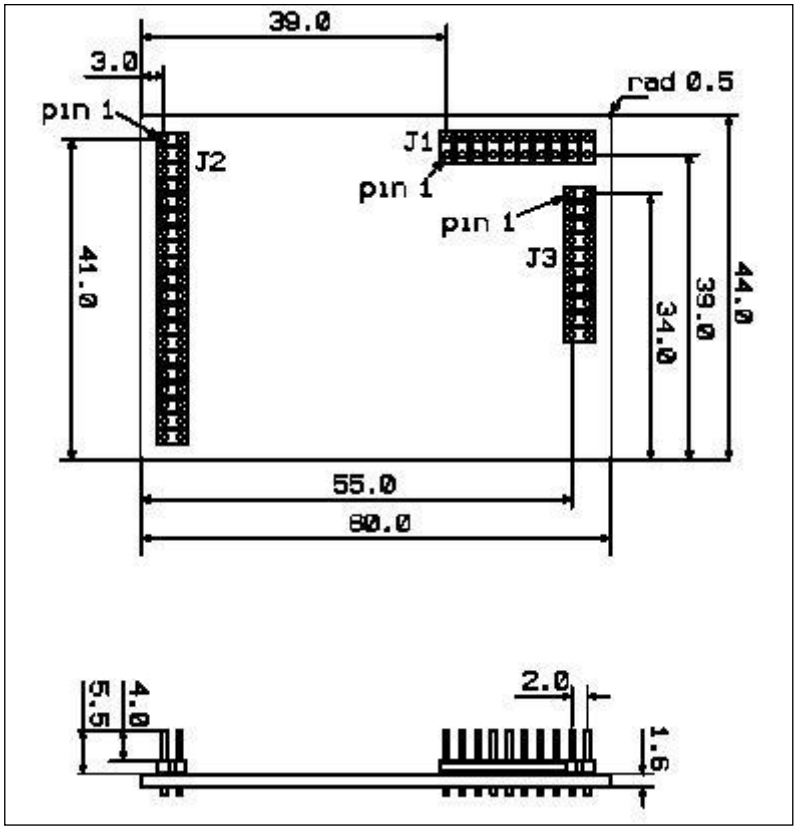

Figure 4 Barracuda Module Dimensions

Notes

1. The protrusion of the connectors through the PCB is not a controlled dimension.
2. The height of electronic components mounted on the Barracuda module varies and Reciva should be consulted before mounting any components, on the application board, within/under the footprint of the module.