Porting Linux to Cortex-M7 microcontroller

Toshifumi NISHINAGA
$ whoami

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Position : Master’s student
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Achievement:

White digital book 「BareMetal で遊ぶ Raspberry Pi」
Internship: FCT, RikenAICS, Fujitsu, AXE
Kernel/VM@Hokuriku organizer
Joined in internship

- **Company**: Fujitsu Computer Technologies (FCT)
- **Period**: two-week
- **Theme**: Porting Linux to Cortex-M7 microcontroller

<table>
<thead>
<tr>
<th>SoC</th>
<th>STM32F746NG</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flash</td>
<td>1-MB</td>
</tr>
<tr>
<td>RAM</td>
<td>340-KB</td>
</tr>
<tr>
<td>D-Cache, I-Cache</td>
<td>4-KB</td>
</tr>
<tr>
<td>External SDRAM</td>
<td>128-bit (64-Mbit accessible)</td>
</tr>
<tr>
<td>Pipeline</td>
<td>6-stage, super-scaler</td>
</tr>
</tbody>
</table>

Ideal

For further information check:
http://www.uclinux.org/

Execution Finished, Exiting

Sash command shell (version 1.1.1)
/> ifconfig eth0 10.0.0.89

oeth_phyMac_synch:eth0 MR1: 0x0000784D
  Link OK: MODER: 0x0000A040
  HalfD
  100BASE-TX

/> inetd

http://opensource.zylin.com/niosuclinux.html
Actually

```
0.010000] Calibrating delay loop... 385.84 BogoMIPS (lpj=1929216)
0.130000] pid_max: default: 4096 minimum: 301
0.130000] Mount-cache hash table entries: 1024 (order: 0, 4096 bytes)
0.130000] Mountpoint-cache hash table entries: 1024 (order: 0, 4096 bytes)
0.170000] devtmpfs: initialized
0.210000] clocksource: jiffies: mask: 0xffffffff max_cycles: 0xffffffff, max_idle_ns: 1911
2604462750000 ns
0.330000] clocksource: Switched to clocksource arm_system_timer
0.570000] io scheduler noop registered (default)
0.570000] STM32 USART driver initialized
0.570000] 40011400.serial: ttyS0 at MMIO 0x40011400 (irq = 17, base_baud = 6250000) is a stm32-usart
0.830000] console [ttyS0] enabled
0.880000] List of all partitions:
0.890000] No filesystem could mount root, tried:
0.900000] Kernel panic - not syncing: VFS: Unable to mount root fs on unknown-block(1,0)
0.900000] ---[ end Kernel panic - not syncing: VFS: Unable to mount root fs on unknown-block(1,0)
55.180000] random: nonblocking pool is initialized
```
Current progress...

- **Done**
  - Add DeviceTreeScript(DTS)
  - Fix STM32 USART driver
  - Fix arch/arm/mm/proc-v7m.S
    - Insert NOP(x4) between “cpsie” and “svc” (cause is 6-stage pipeline ?)
- **TODO**
  - Make tiny rootfs
  - D&I-Cache support
  - 200MHz clock mode support
  - Make DT supported tiny bootloader
  - Cleanup code
Next

- Commit code to community
- Send proposal to Google Summer of Code and process TODO.