Jailhouse Hypervisor for low latency, low jitter HIL systems

Nikola Stojkov / Typhoon HIL

What is demonstrated
A low latency, low jitter, deterministic platform based on Intel Xeon D CPU and Jailhouse Hypervisor, for Hardware in the Loop (HIL) systems. The FPGA is used as HIL's IO interface over the PCIe bus, with bare-metal applications running in the Jailhouse cells.

Hardware Information
Intel Xeon D 1548, Congatec SOM
Xilinx FPGA
Analog and Digital IO

Jan Kiszka / Siemens AG

What was improved
HIL's signal processing capability
✓ Bare-metal applications on x86 using Jailhouse Hypervisor
✓ Flexible software architecture using Jailhouse Hypervisor
✓ 20x times performance increase over ARM Cortex A9 CPU

Flexibility of the system
✓ Possibility for open source HIL platform
✓ Open source Python API interface to Hardware
✓ Rapid control prototyping

Source code or detail technical information availability
Jailhouse Hypervisor: https://github.com/siemens/jailhouse
Typhoon HIL: GitHub repo available soon