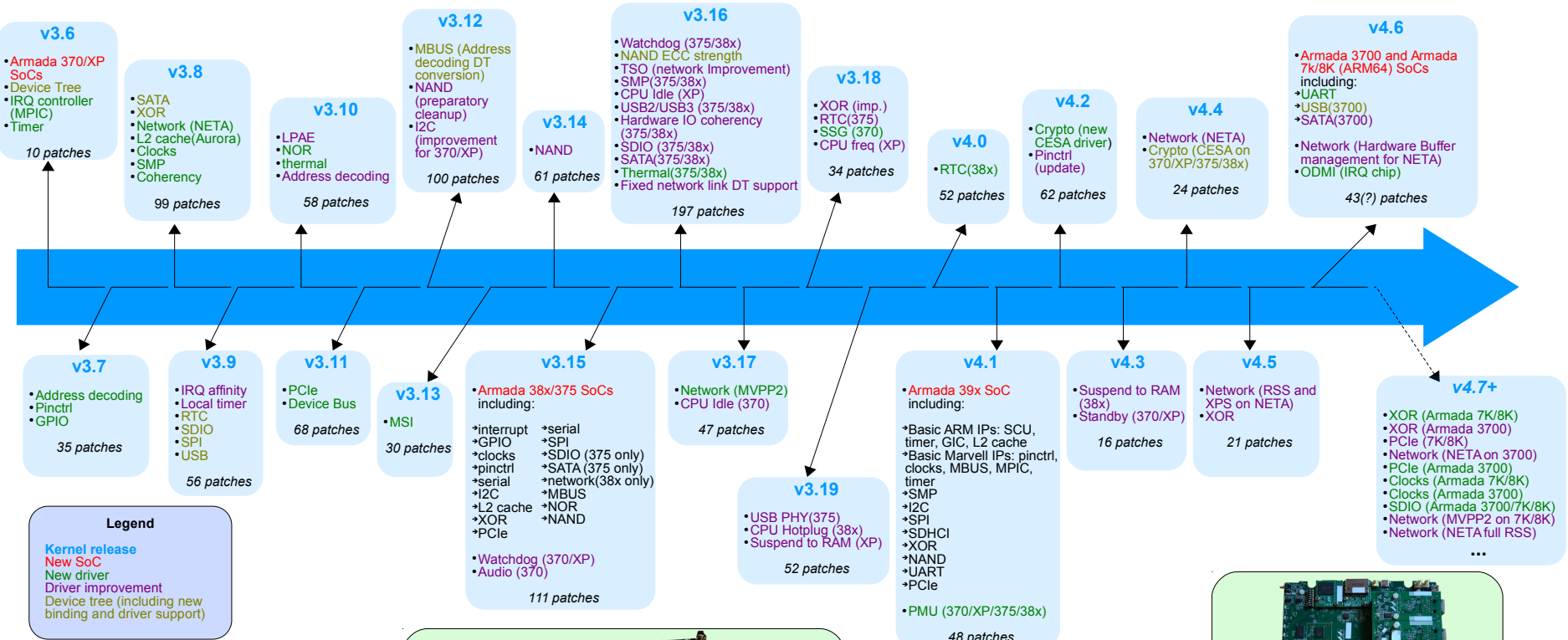





4 years of mainlining effort on Marvell SoCs

Grégory CLEMENT – Free Electrons



Where to find the sources:


- In mainline kernel!
<http://kernel.org>
- MVEBU subsystem:
[git://git.infradead.org/linux-mvebu.git](https://git.infradead.org/linux-mvebu.git)
- Development repository:
<https://github.com/MISL-EBU-System-SW/mainline-public>



Armada 388 GP
Marvell evaluation board:

- Dual Cortex A9@1.6GHz
- 1 PCIe slot
- 4 SATA ports
- 1 USB3 port
- 2 GbE ports
- 2GB DDR
- 2 mini PCIe slots
- 1 SDIO slot
- 2 USB2 ports
- 2 GPIO/interrupts expander on I2C


Everything supported in mainline kernel



Armada 38x ClearFog A1:
SolidRun SBC:

- Dual Cortex A9@1.6GHz
- 2 miniPCIe/mSATA slots
- 1 USB3 port
- 1 SDIO port
- 6 switched GbE ports
- MikroBUS

Everything supported in mainline kernel



Armada 3700 DB
Marvell evaluation board:

- Dual Cortex A53 (64 bits)
- 1 SATA port
- 1 USB3 port

Already supported in mainline kernel

- 1 PCIe slot
- 2 GbE ports
- A SDIO port

Scheduled for the next kernel releases