Table of Content

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WHAT IS A TPMP?

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TPMP IS

- Acronym for Thermo-regulated Power Management Platform
- A power measurement tool (Voltage/Current) for Linux/Android device
- A Hardware Thermal regulation for device under test (Heating or Cooling processor)
- A solution to control all parameters in test environment
- A framework that allows to replay a test suite identically and collect results

TPMP IS NOT

- An option to solve thermal issues on embedded devices
- A thermal policy

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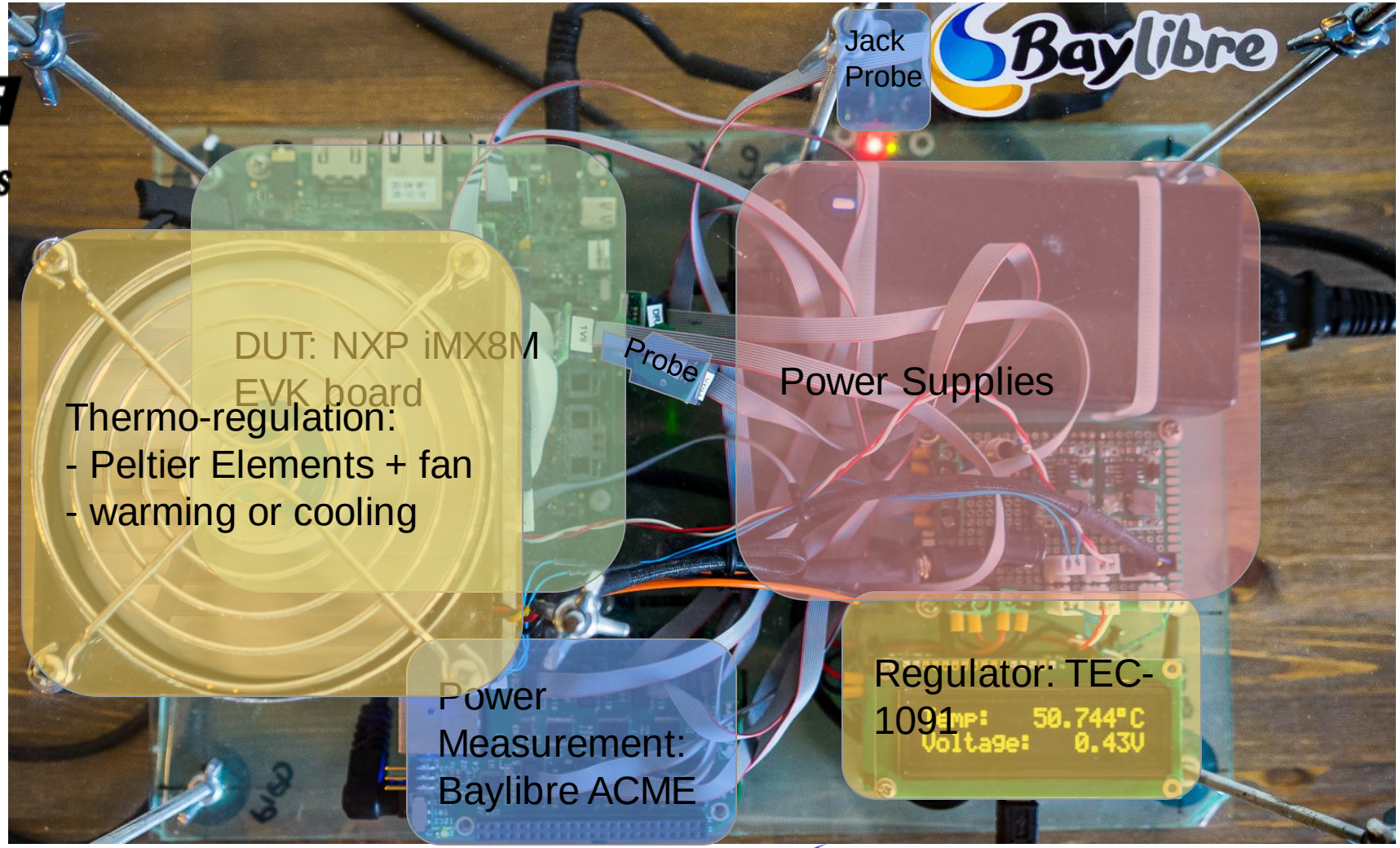
TPMP Overview

- **Thermo regulation control.**
- **Power measurement acquisition.**
- **Test launcher.**
- **Synch-up tasks and store collected data and logs.**
- **Data Post processing**



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HOW IT WORKS?

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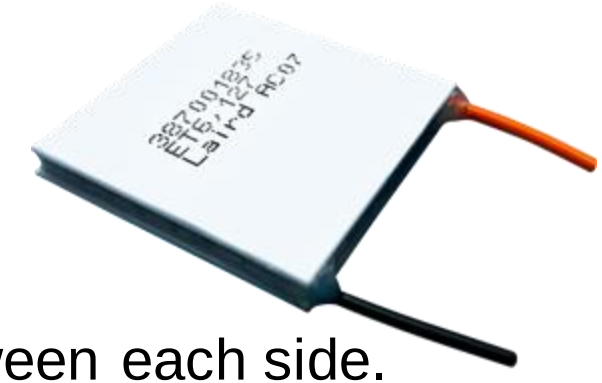
Thermo-Regulation



- Peltier Elements: Laird High Temp Series
  - Direct **conversion of voltage** to temperature difference between each side.
  - Associated to **low noise** fan 3-wire + aluminium heatsink to dissipate calories

- Regulator
  - Meerstetter TEC-1091 + Display DPY-1113
  - Python API: pyMeCom

- Sensors:
  - Thermistor for fan control
  - Pt100 sensor closed to DUT for TEC feedback
  - iMX850MQ On Die sensor loopback performed by software

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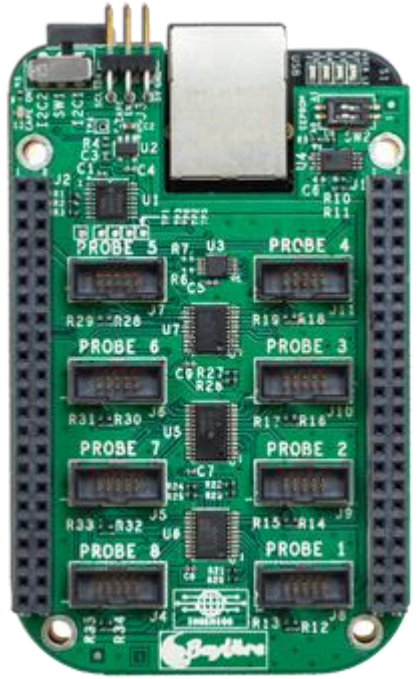
Power Measurement: Baylibre ACME

- The ACME solution comes as an extension for the **BeagleBone** Black (the ACME Cape), designed to provide multi-channel power capabilities to the BeagleBone Black. Up to **2 capes** can be stacked.
- **Jack** Probe to measure total power and perform power ON-OFF cycles
- 5x 2pin HE-10 **power** probe to monitor individual rails. 8probe/cape. Up to 16 probes/Beagle.
- SW: pyacmegraph for **live** capture, pyacmecapture to **store** data for post processing.



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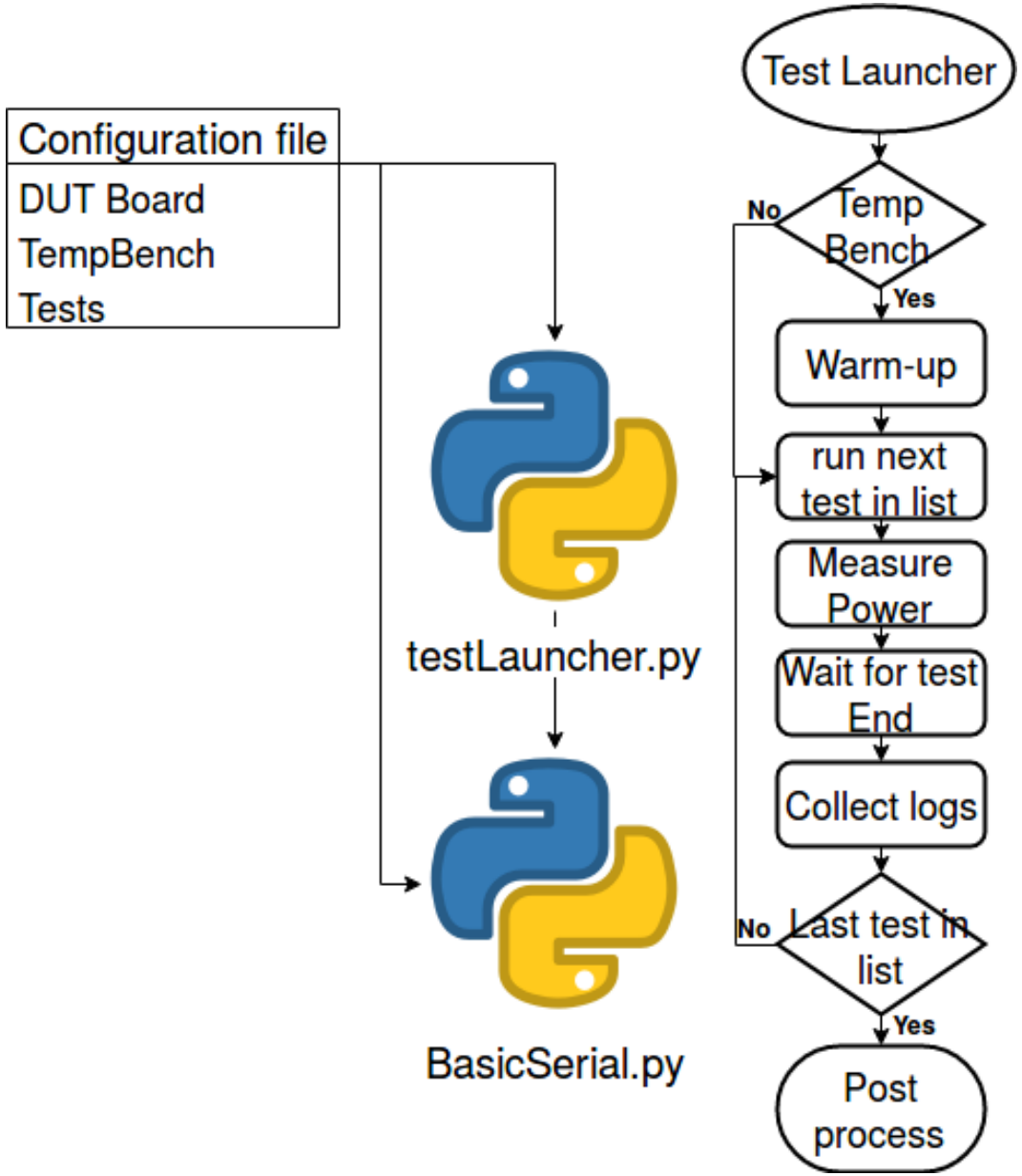
Test Framework

- Common configuration file
- Basic Serial: Interactive
  - Set-temperature, get-temperature
  - Push/pull files
  - Power cycle DUT
- Test Launcher: Automated
  - Sequence operations
    - Start-up device
    - Start test
    - Collect data (Power and test logs)
    - Test teardown and error management
- Source: github/NXPmicro/tpmp_ctrl



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Modularity

- **Terminal** like **interface** available to control the bench **interactively** for development (Test automation optional)
- Test **automation** can be used independently to run tests only, run test + collect power data w/o thermal regulation.
- Communication with DUT relies on **serial port only**: Linux/Android are handled in the exact same way
- Baylibre ACME Ethernet support for **remote control**
- BeagleBone Black **GPIOs** can be driven from the test launcher for additional controls.
- **Open source framework** python3 can be customized for alternative equipment.

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Configuration through common conf file: TEMPBENCH

Warm-up config

Temp Die Target

Temp Fine Tune Parameters

```
[TEMPBENCH]
# path to meerstetter python lib
pyMeComPath = ./lib/meerstetter/pyMeCom/
# id for Meerstetter Peltier controller
peltier_serial_hwid = 0403:6015
#tempTarget = 30
deltaTargetHigh = 10
deltaTargetLow = 4
limitLowHigh = 60
warmUpAuto = True
# launch this test for warmup (optional)
warmUpTest = warmuptest.sh
# target die temperature for testing if commented out,
test launcher will execute tests wo tempcontrol
tempDieTarget = 25
# True: Fine tune temperature at begining of each test
tempFineTune = true
# tempFineTune duration before delta temp is measured for
correction in seconds
TFTRamp = 20
# tempFineTune total duration in seconds
TFTDuration = 50
# in case some tests needs larger duration than normal
for convergence:
# Warning this is just used for timeout calculation this
needs to be consistent with shell script if used
TFTMultiplier = 2
```


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Configuration through common conf file: TESTS

```
[TESTS]
# test timeout in sec
#testTO = 250
testTO = 60
# basic: pseudo terminal full support mini: real terminal
miniterm customized limitted usage testLauncher cannot be used
for now.
termType = basic
# Force board pwrcycle at testLauncher start-up
bootBoardInit = True
# test duration sec (wo temp fine tune duration)
testDuration = 30
#probeDuration = 60
# ACME capture probe duration sec
probeDuration = 20
testList = ["coremark1Core-dbg_time.sh", "coremark1Core-
dbg2_time.sh"]

#prepareBoard = False
# True: use pyacmegraph interface, no report generation, False:
use pyacmecapture with full report generation and logs.
#acmegraph = True
acmegraph = False
# used to power cycle board
acmecliPath = /home/nxf44606/Baylibre/ACME/CLI/acme-cli/
# acme name in /etc/hostname
acmeName = baylibre-acme-ptec-jn.local
#change with path of pyacmegraph.py on host (used only when
acmegraph = True)
pyacmegraphCmd = /home/nxf44606/Baylibre/ACME/GRAPH/pyacmegraph/
pyacmegraph.py
#change with path of template file .acme
pyacmegraphTemplate = /home/nxf44606/Baylibre/ACME/GRAPH/
pyacmegraph/config/VDD12345678NXP.acme
#Force shunt values (might not be needed any longer with latest
acme sw revision)
pyacmegraphShunt = --shunts=10,50,20,50,50,50,50,50
# directory to store logFiles on target
logFilesPath = ./logFiles/
# location of test files on target. path related to
boardConnectPattern
```

Test Timeout

Test Duration

Probe Duration

Test list

Results

Reboot

Path to local tools

```
# location of test files on target. path related to
boardConnectPattern
testPath = ./
# path to pyacmecapture used to probe power
pyacmecapturePath = /home/nxf44606/Baylibre/ACME/CAPTURE_CSV/
acme-utils/pyacmecapture/
#Power rails in same order as probe connection
probeList =
["VBAT","VDD_ARM","VDD_SOC","VDD_DRAM","NVCC_DRAM","VDD_1V8",
# Name of result dir
resultsDir = Testcleanuptrial-25C
# pwrcycle after each test completion. If this is not done,
correct teardown should be done to ensure consistent
measurements
rebootAfterEachTest = True
# exitOnLauncherEnd = True: exit testlauncher when all tests
are completed/exitOnLauncherEnd = False: stay connected to
board at end of test for further debbug
#exitOnLauncherEnd = True
# create a zip file with results
zipresults = True
```


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Configuration through common conf file: DUT BOARD, MAIL

```
[TESTBOARD]
# id for board connected through serial
board_serial_hwid = 10C4:EA70
# serial baud rate
baud = 115200
boardConnectPattern = /unit_tests/autotest#
# recomended zmodem (needs to be installed on target)
otherwise txtCopy (No sw needed on target but limited to
txt files only, no binary and no integrity check)
copyMethod = zmodem
;copyMethod = txtCopy
# pattern detected at board boot up to enter login pwd
loginvite = evk login
# root pwd
boardpwd = root
```

Test path on DUT

Login

Host Path to test dir for copy

Send result by mail

```
[SHELL]
#Path of files to copy on board
#cpdir = ../shell
#avoid copy at each reboot need to implement configure_board
on first reboot only
cpdir = ../fake

# Send test report automatically by email to recipient list
[MAIL]
#tested with gmail, need to modify security, allow less
secure apps: https://myaccount.google.com/lesssecureapps
smtp = smtp.gmail.com
# replace with your account password
#login = password
fromaddr = jerome.neanne@nxp.com
# comment toaddr to avoid sending mail
#toaddr = ['jerome.neanne@nxp.com', 'pascal.mareau@nxp.com',
'john.doe@nxp.com']
#toaddr = ['jerome.neanne@nxp.com']
```


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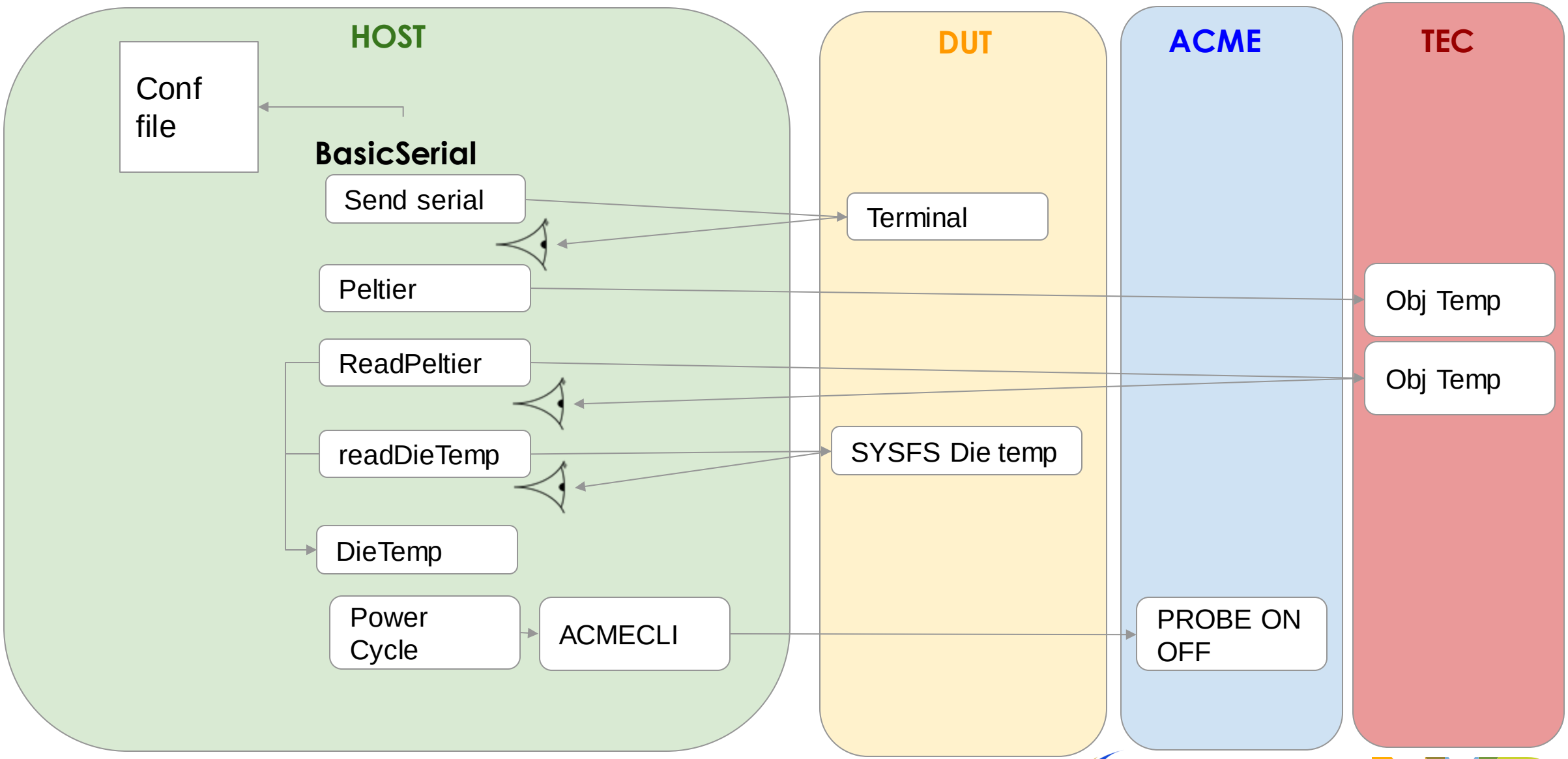
Framework architecture overview interactive mode



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Tests formatting

```
#!/bin/bash
duration=$1
uname -a
echo "BoardID: "
/unit_tests/memtool -32 0x3035C410 1
/unit_tests/memtool -32 0x3035C420 1
/unit_tests/autotest/OPP-setup.sh
echo "CPU0 online: "
cat /sys/devices/system/cpu/cpu0/online
echo "CPU1 online: "
  .
  .
  .
echo "clk_summary"
cat /sys/kernel/debug/clk/clk_summary
echo "--------------------TEST start: $0 ----------------------------"
cd /unit_tests/autotest/kpa_coremark_scripts;
/unit_tests/autotest/kpa_coremark_scripts/QX_coremark_run.sh &
ps
echo "--------------------FINE ADJUST TEMP----------------------------"
/unit_tests/autotest/print_temp_time_s.sh 100 2
echo "--------------------POWER PROBE Start: $0 ----------------------------"
/unit_tests/autotest/print_temp_time_s.sh $duration 2
echo "--------------------POWER PROBE End: $0 ----------------------------"
/unit_tests/autotest/teardownCM.sh
cd /unit_tests/autotest;
```

Test Log

Keywords

Launch test

Optional trace

Cleanup

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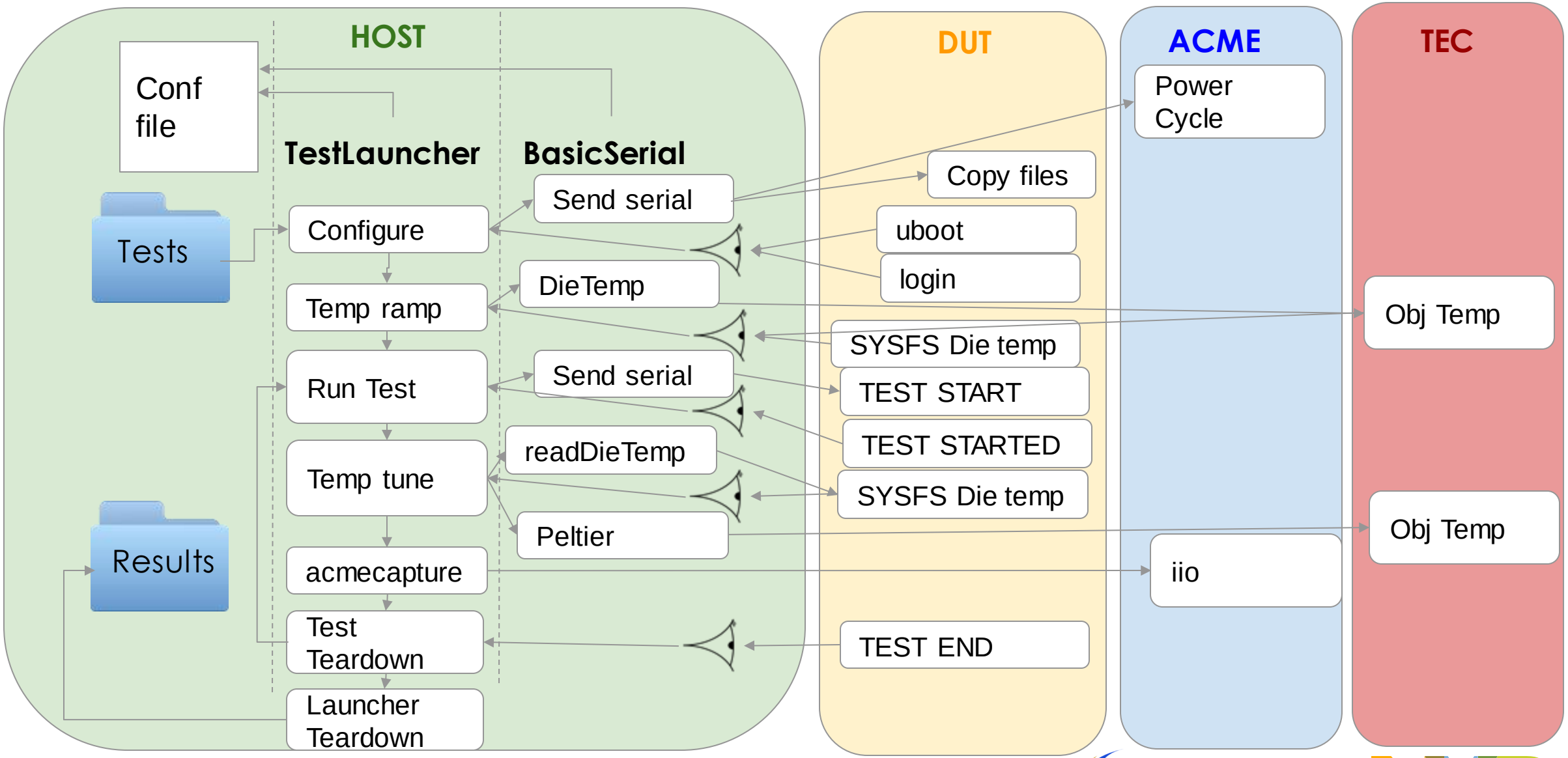
Framework architecture overview Automated mode



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Want to try it?

- Come to see more & try at ELC Technical Showcase
- When? Tuesday October 29 from 17H45
- Where: Forum 4/5

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WHY DO WE NEED

OTHER OPTIONS?

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Other thermal forcing lab tools

Thermo stream

[ATS-545M Datasheet]

Thermal chamber

[DY16T Technical data]

Thermal forcing by conduction

[MAX TC G4]

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TPMP VS traditional solutions (1/2)

	TPMP 	Thermo-stream ATS-545M 	Chamber ACS PY16T 
Size LxWxH (cm)	30x20x20	61x72x108	46x54x68
Weight (Kg)	<3	236	60
Temp range(ºC)	10:125	-80:255	-35:130
Accuracy(ºC)	∓1	∓1	∓1
Noise (dBA)	<15	<65	<52
Power	24V-6A	230V-30A	230V-4A
Transition rate	1ºC/s heating 0.5ºC/s cooling	18ºC/s	4ºC/min
BOM ($)	~1 000	~40 000	~4 000

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TPMP VS traditional solutions (2/2)

	TPMP 	MAXTC G4 	FlexTC 
Size LxWxH (cm)	30x20x20	61x50x36	42x32x22
Weight (Kg)	<3	52	22
Temp range(ºC)	10:125	-40:175	-40:155
Accuracy(ºC)	∓1	∓0.5	∓0.5
Noise (dBA)	<15	<55	<45
Power	24V-6A	230V-10A	230V-10A
Transition rate	1ºC/s heating 0.5ºC/s cooling	75ºC/min	75ºC/3min
BOM ($)	~1 000	~30 000	~20 000

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WHY DO WE NEED

PHYSICS!

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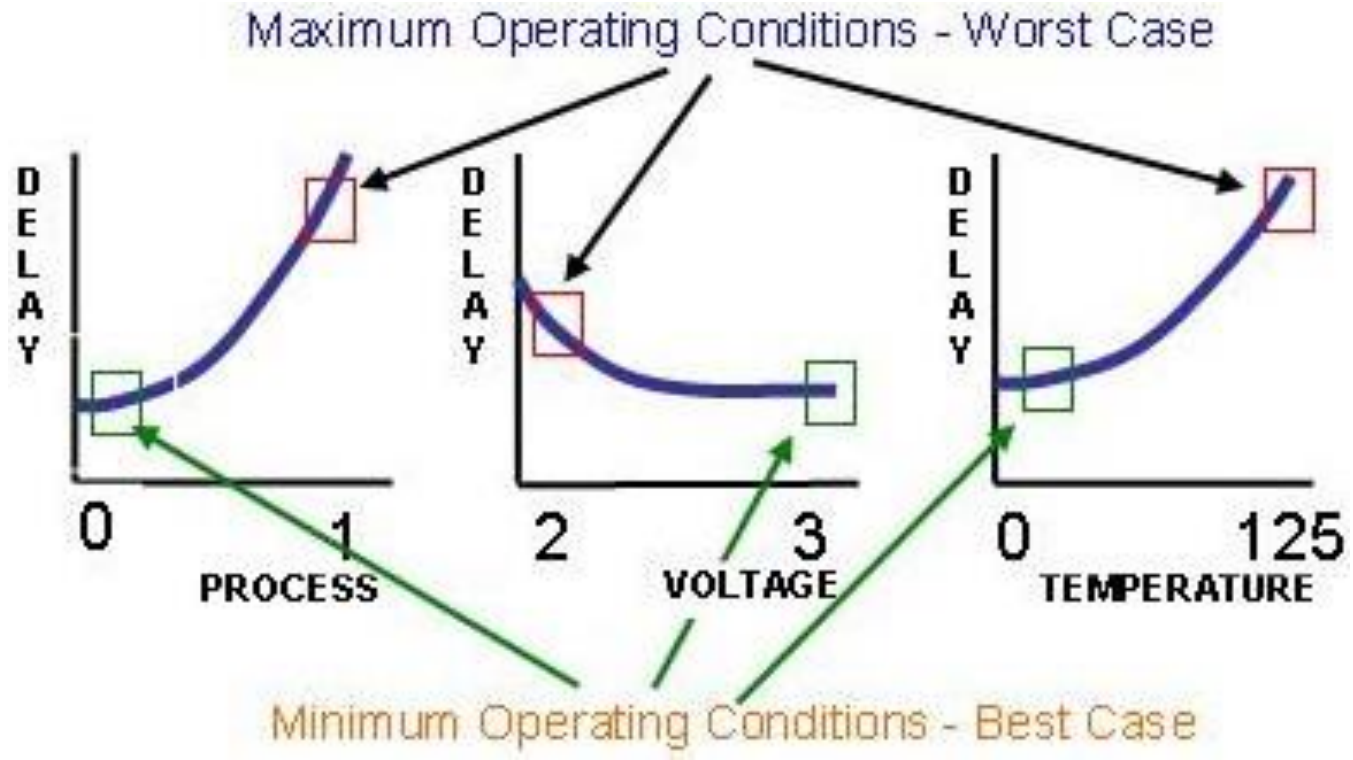
Definitions: Process Performance

- Process: Account for deviation in the fabrication process
- Performance: Signal propagation delay on silicon converted to clock frequency (MIPS). Higher mobility Lower delay higher perf.
- PVT: Process, Voltage, Temperature



Higher Voltage = Higher Perf

Higher Temp = Lower Perf

Process ?

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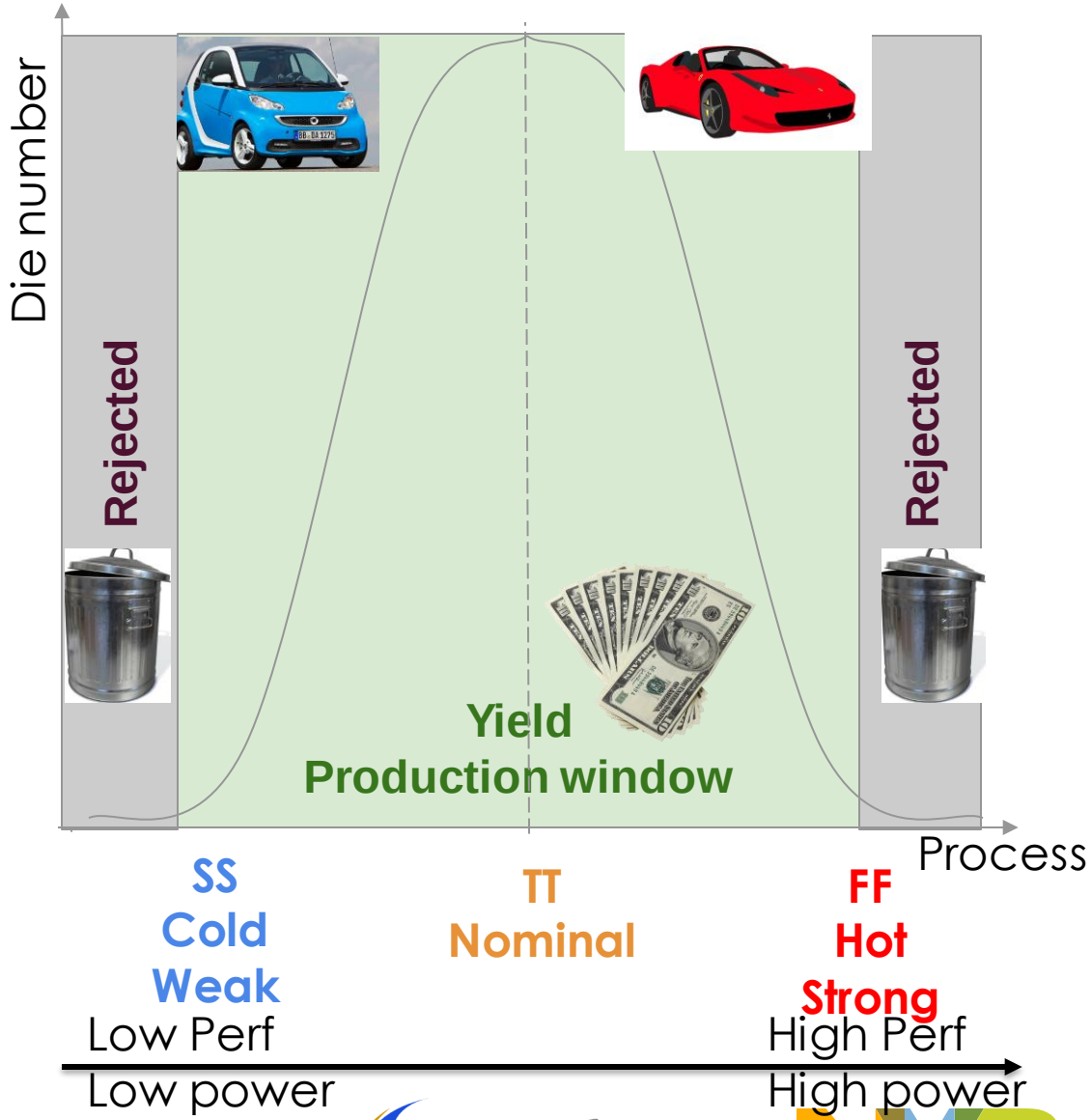
Silicon characterization glossary

- Split lots: wafer fabricated with process parameters adjusted to extreme
  - Fast/FF/Hot: High performance, high power
  - Slow/SS/Cold: Low performance, low power
  - Typical/TT/Nominal: process centered
- Process corner:
  - Best Case: fast Process, high Voltage, low Temp
  - Worst Case: slow Process, low Voltage, high Temp



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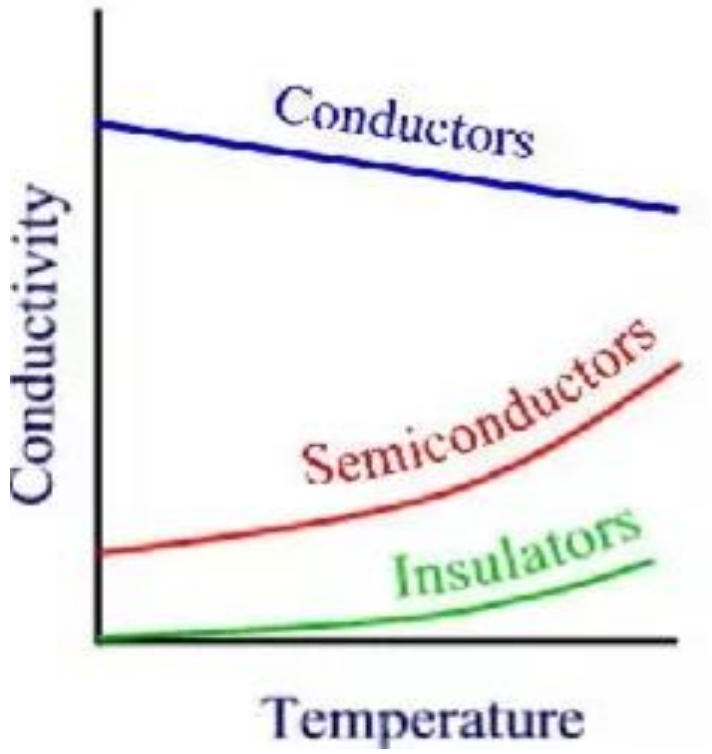
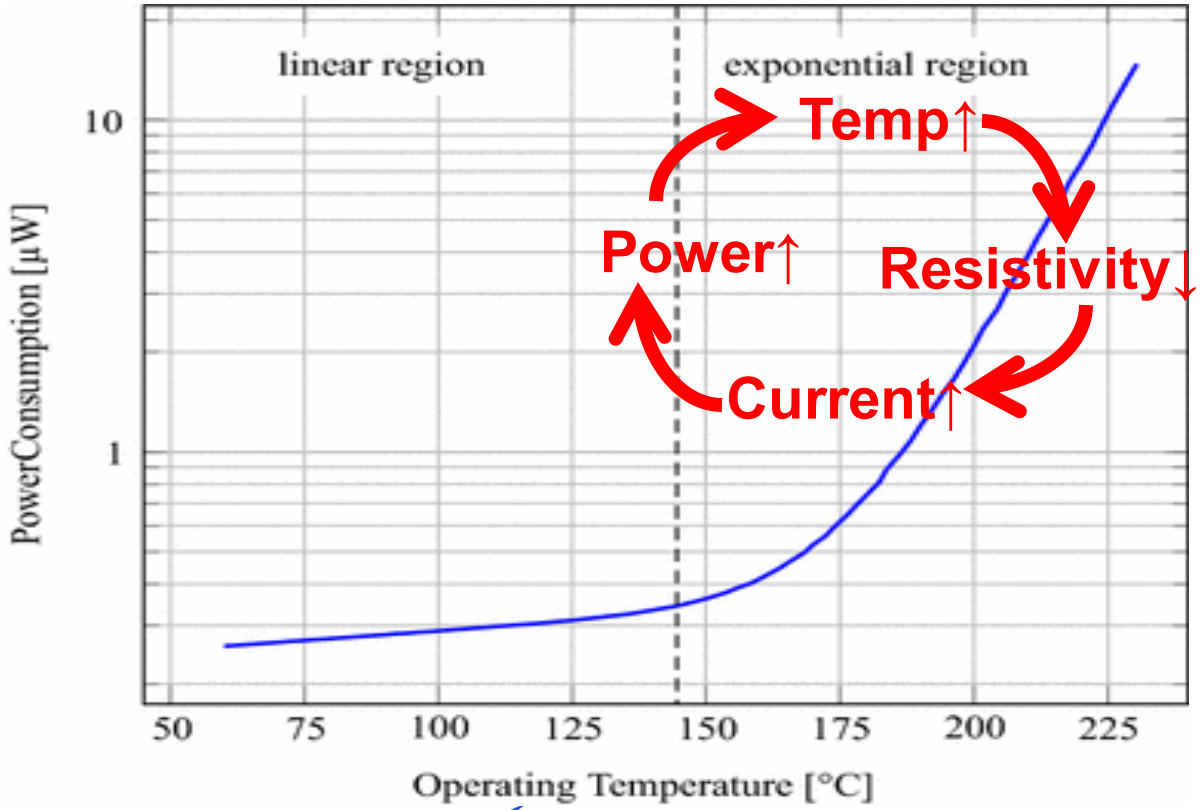
How High Temperature affects silicon

- Mobility decreases with Temp: **Lower Performance**
- Carrier number increases with Temp
- Conductivity increases with Temp: **Higher Power**
- High Temp: Lower Perf Higher Power





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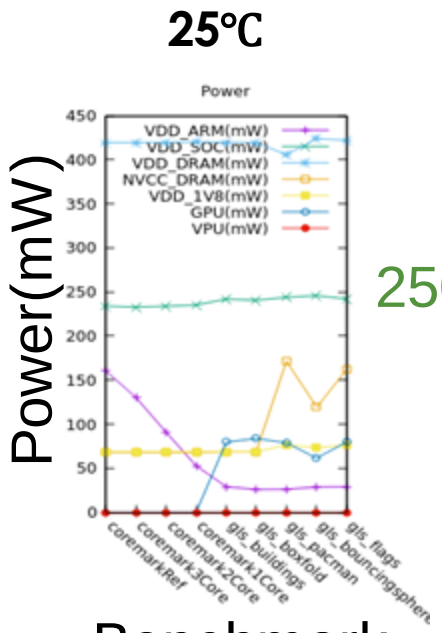
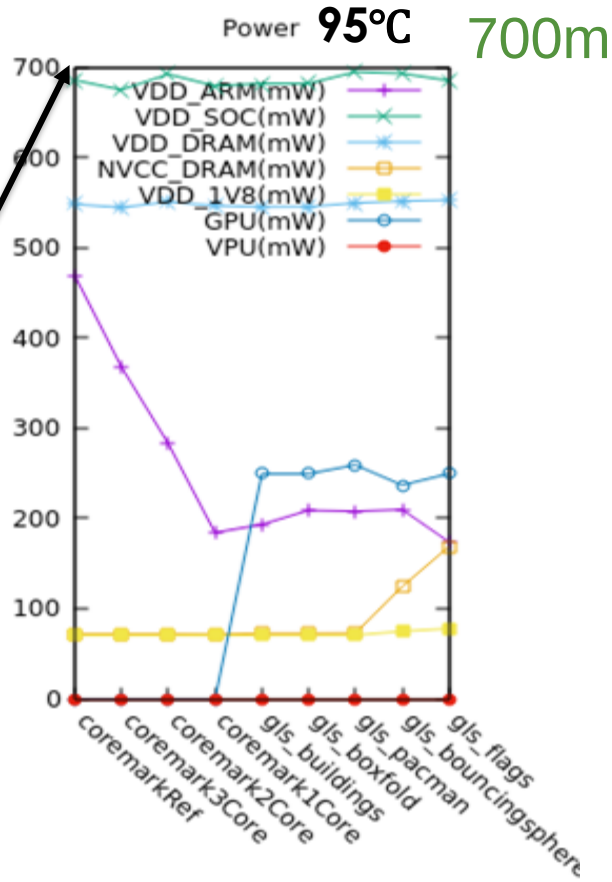
Characterization result charts for one board at same scale

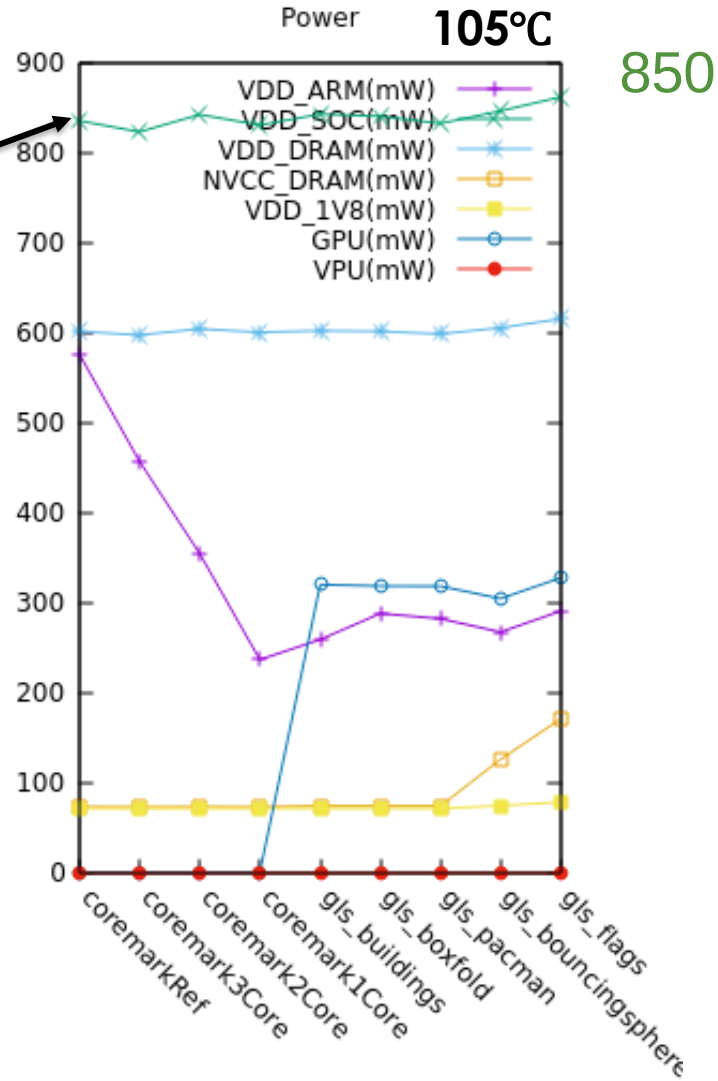
Temperature impact on SOC rail:
3.5x factor



250mW



700mW



850mW

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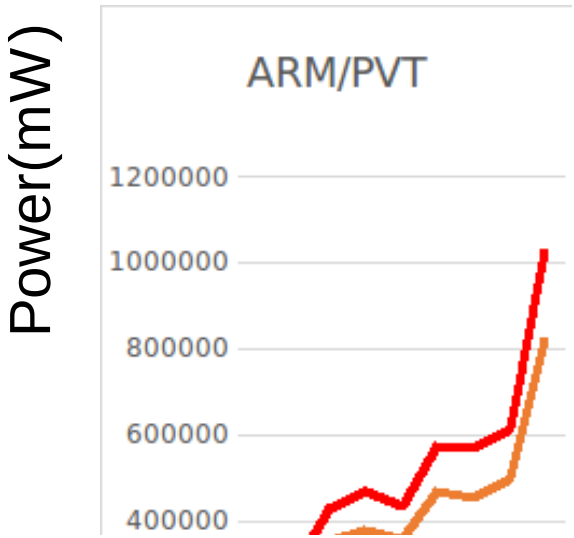
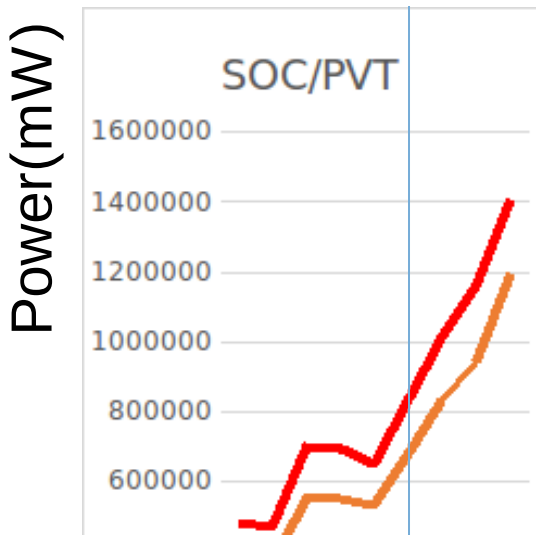
Characterization across boards for one use case (coremark)





MAJOR IMPACT OF TEMPERATURE AND PROCESS ON POWER MEASUREMENT. THERMAL FORCING IS MANDATORY TO ENSURE RELEVANT MEASUREMENTS

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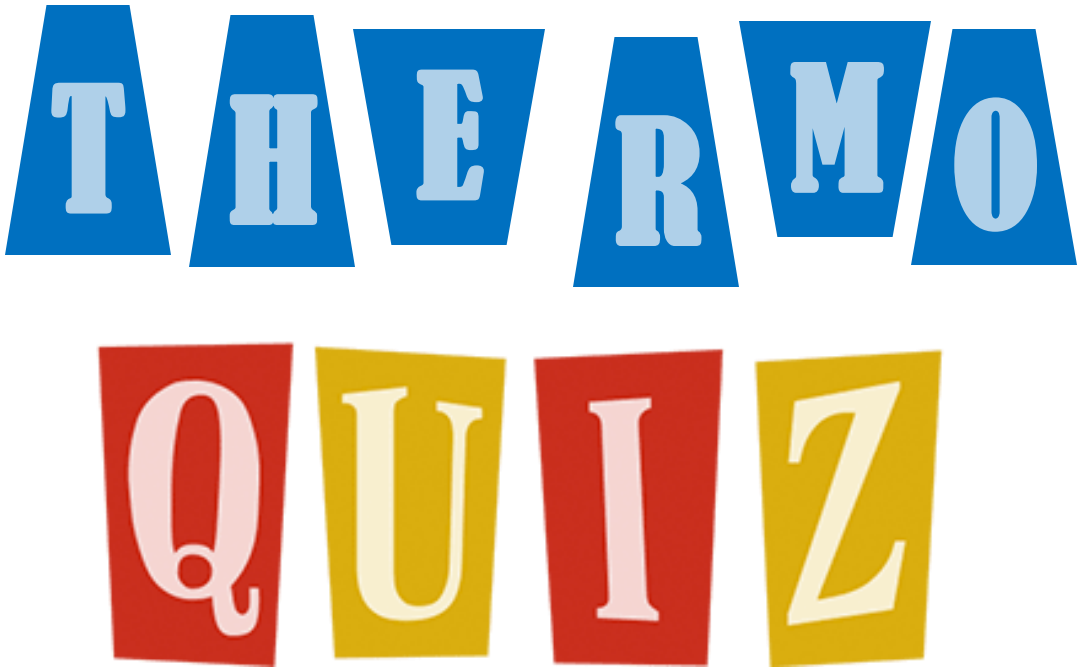
Thermal Quizz

[Go to TPMP quizz]



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WHO NEEDS?

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WHO needs a TPMP

- Characterization engineers
- Industry working on products where power cycle/measurement and temperature conditions make a difference: IC, battery…
- Product engineers working in aging tests and/or worst case conditions
- Power management optimization team.
- Power CI.

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A TPMP
WHEN & WHERE?

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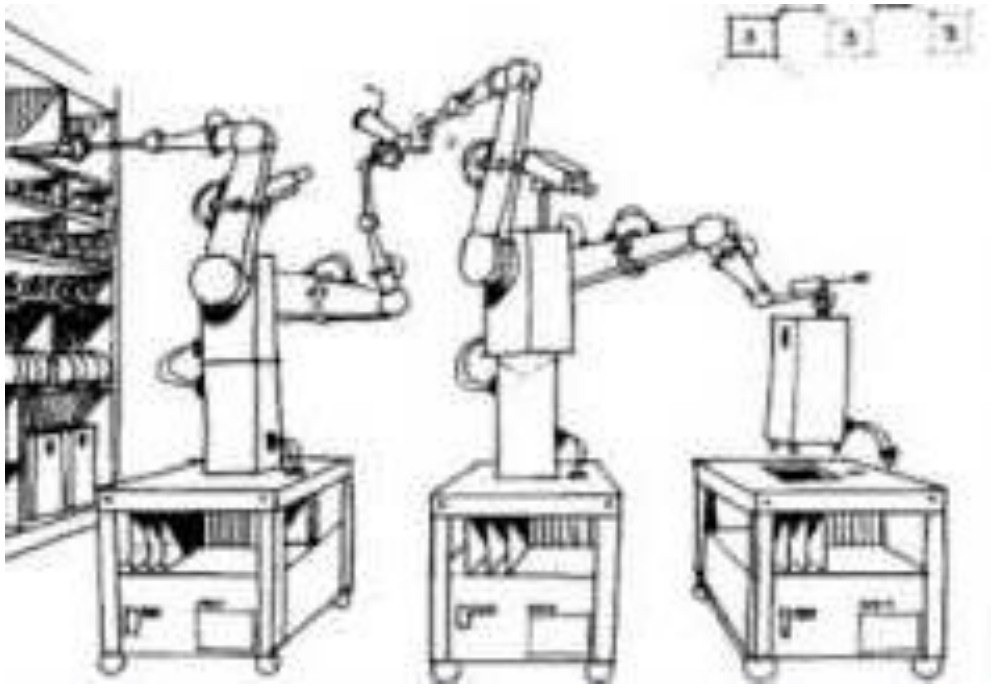
Why thermoregulation is a key element in a power CI?

Replicating !



- Silicon is sensitive to PVT:
  - P&V are fixed by construction
  - Only temperature can be controlled.

- Die Temperature is affected by:
  - Environment conditions
  - Device load
  - Previous activity on the platform (Thermal inertia). Test suite sequencing can impact the result of single test measurement.

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Why thermoregulation is a key element in a power CI?

- High temperature → Higher power for same test: Test Full Steam
- Worst case Power + Worst case Delay: More prone to show failures.
- Aging: Forcing temperature cycle will stress the system in a different way.
- Comparing result at low temperature and high temperature will allow to discriminate temperature related issues.

Measure Worst case!

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Why thermoregulation is a key element in a power CI?

Detect hidden issues invisible at room temp!

- Higher temperature → Higher currents → IR Drop: Potential electrical issues can be detected.
- Assess Thermal policy effects (Power/Performance/Behavior)
- Assess impact of other system components sensitivity to Thermal (ex: DDR self-refresh rate increase)
- Detect and discriminate timing issues that would appear only at high temp (hold violation)

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Why thermoregulation is a key element in a power CI?

Adjust parameters!

- In a CI Farm with N boards:
  - Power measurement depends on the board (Process variation)
  - Different Run of same test on different boards cannot be compared
  - Thermoregulation provides **a way to calibrate devices**

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WHAT'S NEXT?

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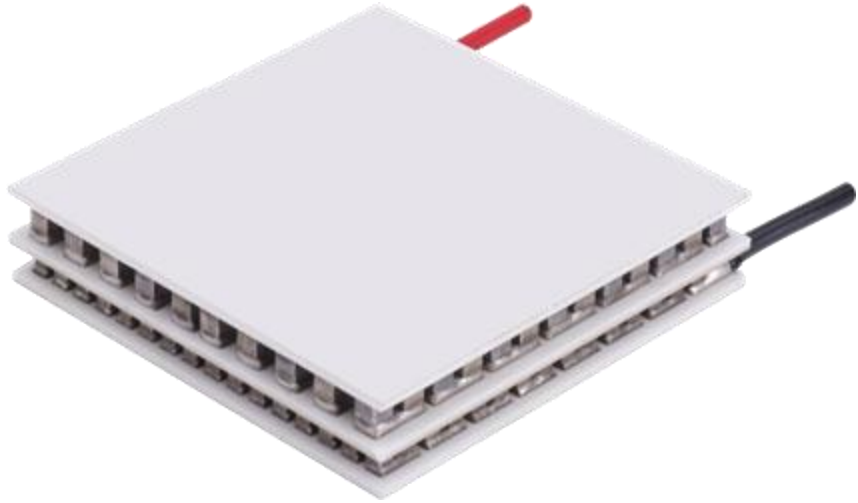
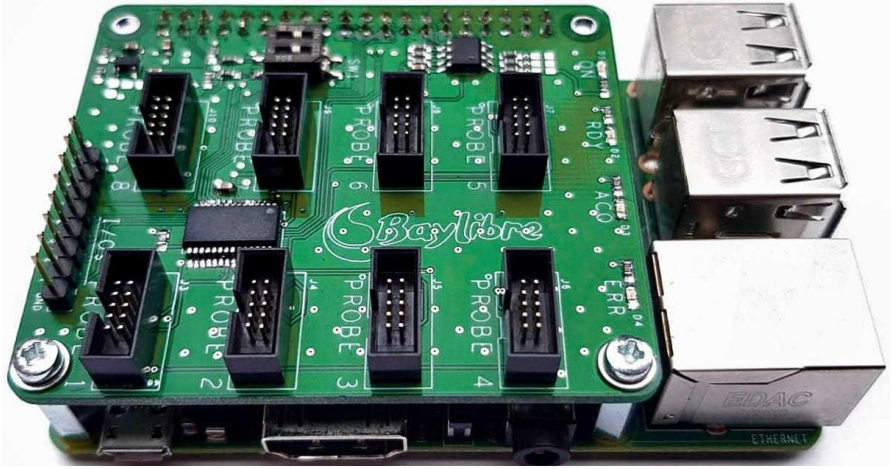
TPMP HW Evolutions (1/2)



- New Peltier element reference used for enhanced performance: in house MultiStage version. MS2-192-14-20-11-18 Better Stability and better performance at low temperature (0°C)

- Baylibre ACME raspberry Hat:
  - Standard connector
  - Lower price



- USB type-C full support
  - ON-OFF box
  - File transfer with remote connection control

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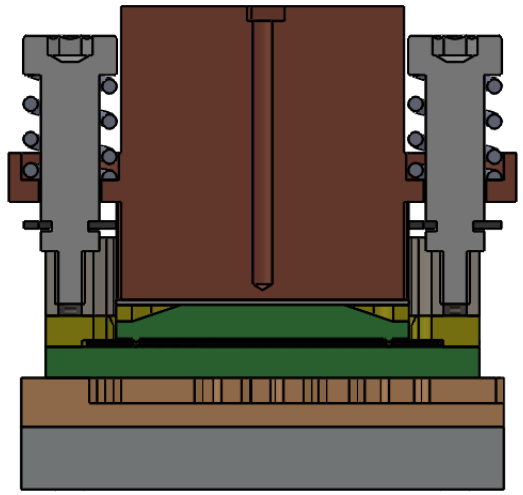
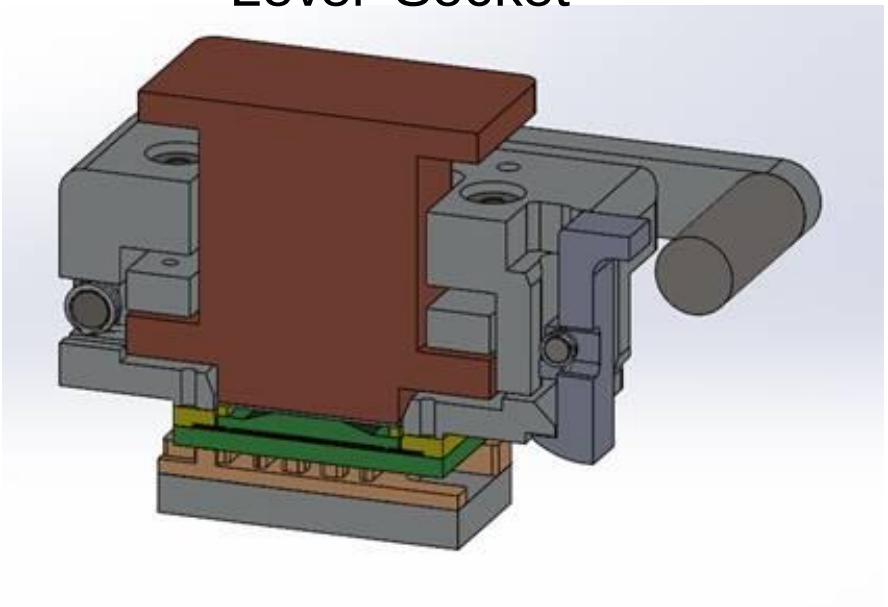
TPMP HW Evolutions (2/2)

- Development of a dedicated socket optimized for thermal transfer efficiency and enabling to swap die:

Swivel Socket



Lever Socket



- New casing

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TPMP Next step SW

- Current implementation relies on a custom Framework that was developed in a POC mode for characterization activity.
- Custom Framework does not provide all the features supported by standard “state of the art” CI Framework.
- TPMP control software should be refactored to expose Thermoregulation feature as an additional instrument for standard CI framework
- A plug-in development for ARM Workload Automation is under study.

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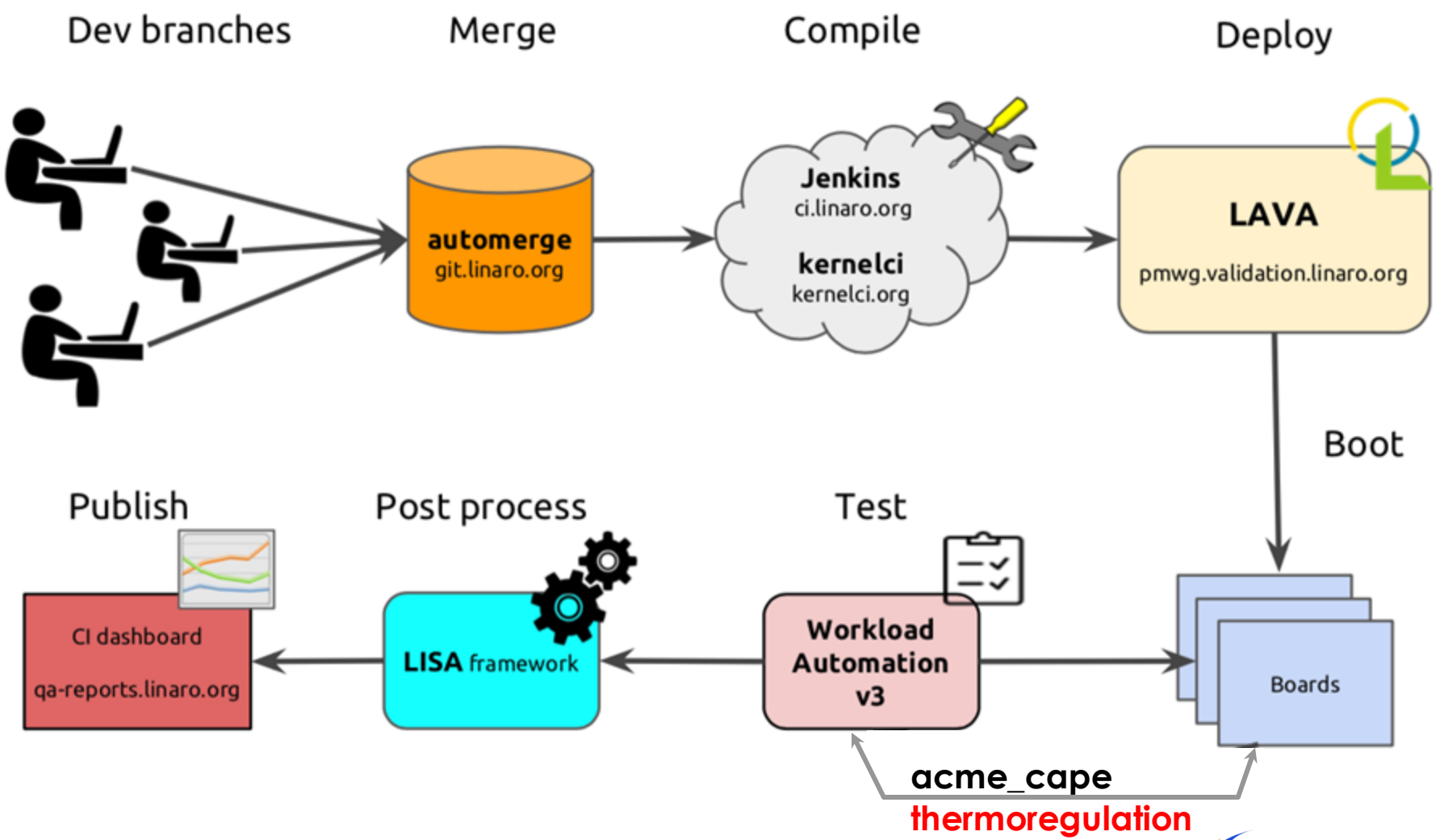
Standardized Thermoregulation for power CI



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Custom solution vs standard

Feature	TPMP	WA	Comment
Merge Dev Branch	✗	✓	Build and flashing not supported in current TPMP implementation
Build	✗	✓	
Kernel CI	✗	✓	
LAVA	✗	✓	
Test Launcher	✓	✓	
Power Measure	✓	✓	
acme_cape	✓	✓	Enhance WA with pyacmecapture instead of IIO capture
Thermoregulation	✓	✗	Develop additional instrument Plug-in
Post Processing	✓	✓	Custom scripts vs LISA framework + publication

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DIFFICULTIES

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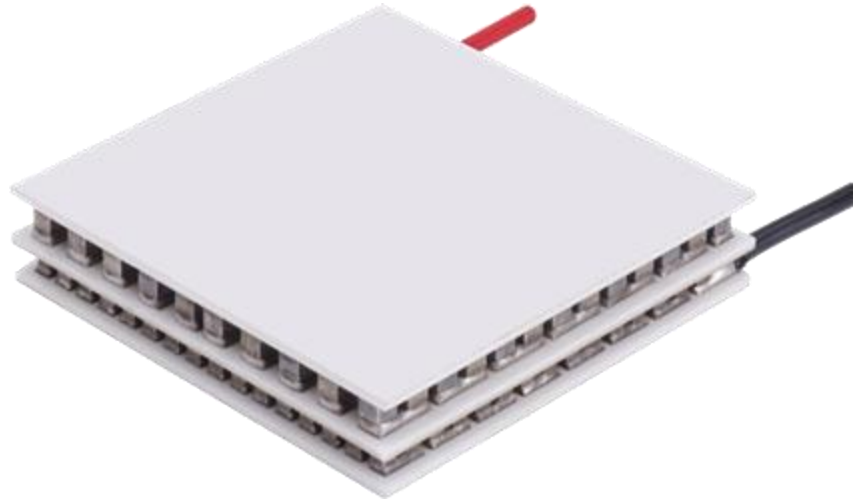
Issues Resolved during development (1/3): Temp Range



- Sustain High Temperatures with Peltier Elements
  - Issue: Regular Peltier collapse after 100°C, higher temperature is destructive
  - Solution: Use High Temp parts

- Cover the whole temperature window: 25°C to 105°C
  - Issue: For some DUT, the power to deliver is over the Peltier characteristics limits.
  - Solution: Move to 24V power supply (full Voltage Range) + Stack 2 Peltier elements

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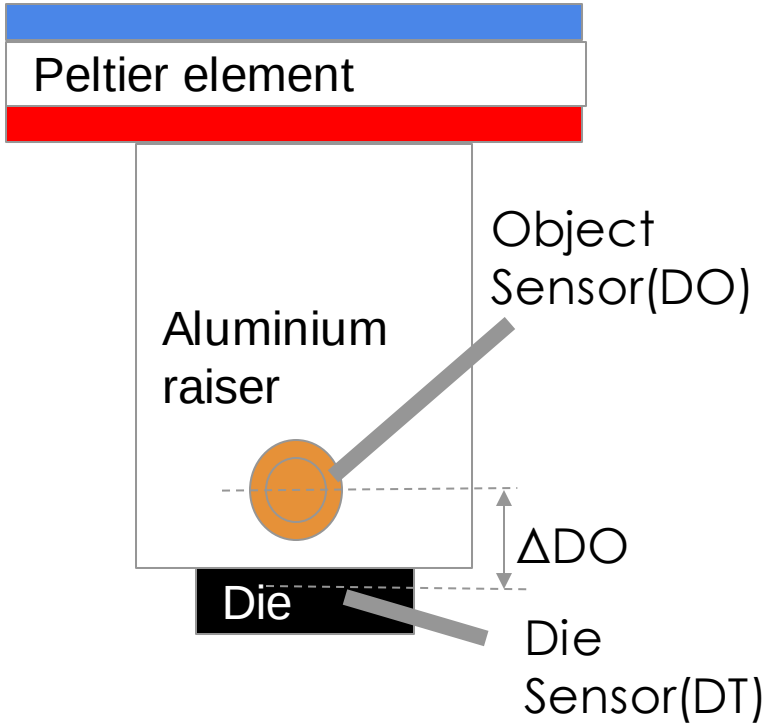
Issues Resolved during development (2/3): Accuracy & Reliability

- Die Temperature accuracy ±1°C
  - Issue: Delta Object sensor die depends on board (Process/Dissipation) and temperature range
  - Solution: SW Close loop with On Die sensor for temperature convergence



- Low Temperature can be destructive
  - Issue: below 20°C condensation starts appearing on the metallic raiser... It will irreversibly damage the board as soon as water touch the board.
  - Solution: Protect metallic surfaces with Silicone tape

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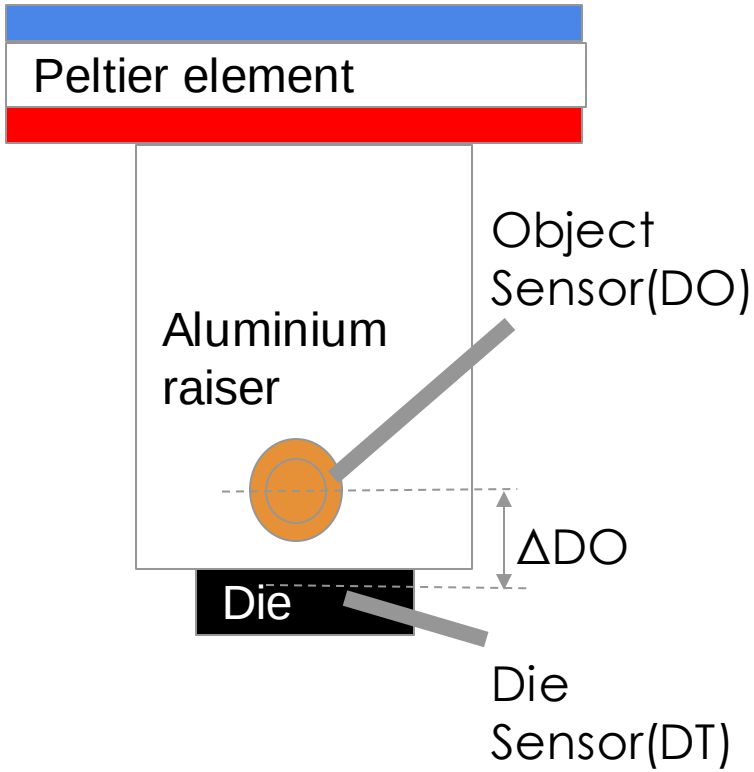
Issues Resolved during development (3/3): Techniques for non intrusive thermoregulation

- Temperature fine tune:
  - Objective: Compensate **ΔT** due to **Test load** variation.
  - After ramp-up completion, TPMP operate in a linear range. TDie - TObject: ΔDO < 5°C
  - Measure Die temp: TD calculate delta to Target ΔDT
  - ΔDT is reported directly to **compensate DT variation.**

- Log capture:
  - **Minimal interaction** with serial link during capture
  - Dmesg is copied to file after test completion
  - Serial log is captured on the host side
  - Capture window ends before test completion and sync message send to host



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ACHIEVEMENTS

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Achievements: Success stories at NXP

- 10 TPMP for different iMX8 flavor delivered and in production
  - Used for OPP characterization
  - Used by validation team for power measurement campain
  - Used by Power Optimization team, soon in power CI.

- Framework used in aging test to detect and reproduce rare issues happening after days.

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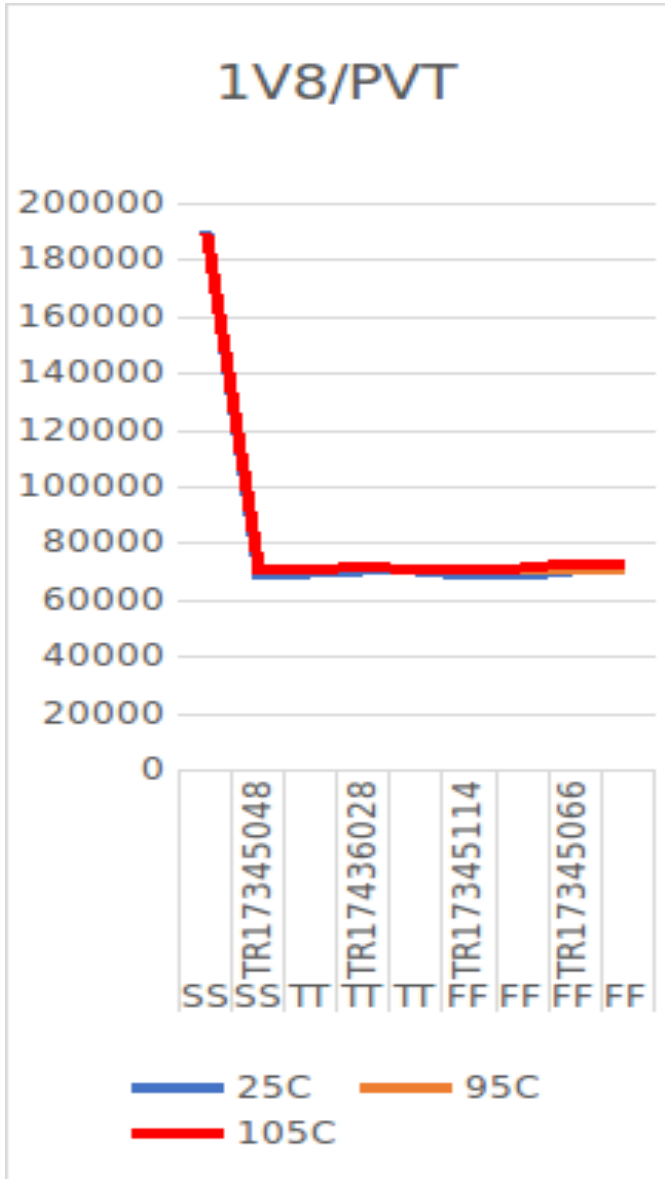
Baylibre NXP

Achievements: Success stories at NXP

- Successfully used to reproduce then analyze performance issues happening at high temperature only.

- Detect board issue while no behavioral impact is visible



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BACKUPS

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Thermo stream

ATS-545M Datasheet

PERFORMANCE:

Temperature Range*

-75 to +225°C (50Hz)

-80 to +225°C (60Hz)

No LN_2 or LCO_2 Required

Transition Rate*

-55 to +125°C, approx. 10 seconds or less

125 to -55°C, approx. 10 seconds or less

System Airflow Output*

4 to 18scfm (1.9 to 8.5 l/s) Continuous

* under nominal operating conditions
ultimate low temperatures (±1°) achieved at 12scfm

FEATURES:

- **Frost Free Feature**
  dry air purge for tester interface, prevents condensation: 0.5 to 3scfm (0.25 to 1.5 l/s)

- **ECO Friendly Feature**
  Heat Only Mode
  reduces power usage when cold temperatures are not used

- **Fully Adjustable Thermal Head**

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Thermal chambers

	MODEL	DY16 T	DY60 T(C)	DY110 (C) [1]	DY200 (C) [1]
Useful capacity (l)		16	59,5	110	206
Internal dimensions approx. (mm)	Width	310	350	548	601
	Depth	230	340	447	541
	Height	206	500	447	634
External dimensions approx. (mm)	Width	465	630	877	927
	Depth	541	970	1080	1379
	Height	685	1180	1434	1794
Temperature range (°C)	Basic	-35...+130	-40...+180	-40...+180	-40...+180
	C model		-70...+180	-70...+180	-70...+180
Temperature fluctuation (K)		±1	±0.1...±0.3	±0.1...±0.3	±0.1...±0.3
Temperature changing rate Heating [4-5] (K/min)	Basic (-40/+180°C)	4,5 (-35/+130°C)	3	3,2	4
	C model (-70/+180°C)		3	3,2	4
Temperature changing rate Cooling [4-5] (K/min)	Basic (+180/-40°C)	3,5 (+130/-35°C)	3	4	4,5
	C model (+180/-70°C)		3	2,8	3
Humidity range (%) (τ=-3/+93°C) [2]				10...95	10...95
Temperature range for climatic test (°C)				10...95	10...95
Humidity fluctuation (%)				±1...±3	±1...±3
Maximum thermal Load (W) [3]	Basic T=+25°C	250	250	350	2300
	C model T=+25°C		250	500	1500
Rated power (kW)	Basic	0,7	2,0	3	6
	C model		2,3	3,7	7
Rated current absorption (A)	Basic	4	9	16	10
	C model		11	16	12
Weight (kg)	Basic	60	210	350[6]	485
	C model		230	360[6]	545
Sound pressure level dB(A) [3]	Basic	52	57	52	53
	C model		59	52	59
Supply voltage (Vac)			230V ±10%/50Hz/1 + G		400 V ±10%/50Hz/3 + N+ G

1. for Temperature only version add the suffix T - 2. τ= +4°C/+93°C for continuous test - 3. measured at 1 m distance in front of the unit, free field measurement - 4. according to IEC 60068-3-5 and IEC 60068-3-6 - 5. The performance data refer to +22°C ambient temperature, 230V or 400V nominal voltage, without specimen - 6. value without supporting table

DY16T Technical data

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Thermal forcing by conduction

System general

Temperature range	-70°C to +175/200°C
Temperature accuracy	±0.5°C
Typical transition rates	25°C to -40°C in ~<2min 125°C to 25°C in ~<2min
Temperature sensor	Tcase PT100 thermistor K-type thermocouple Thermal-diode through ethernet port Thermal-diode through analog port Ethernet (TCP/IP)
System indicators and failsafes	Thermal head over-temperature fan operation, cooling unit operation
DUT pressure force	2 - 100 Kg/Force
DUT dimensions	≥ 2 x 2 mm
DB rating	55 dBA
MTBF	70,000 hr

Mechanical dimensions

System enclosure mm / inch	L) 610mm x (W) 505mm x (H) 365mm (L) 21.8" x (W) 17.7" x (H) 11.8"
System weight	52 Kg
Thermal head (mm)	80mm diameter
Thermal head hose	2 meter (6.5ft) standard

System requirements

Electrical	220/230/240 VAC ±10% 50/60 Hz, single phase, 10A max.
Purge	0.2-0.6[MPa] dry air/ dry Nitrogen
Ambient temperature	5°C to 35°C (40°F to 95°F)
Ambient humidity	20% to 95% RH

MAX TC G4

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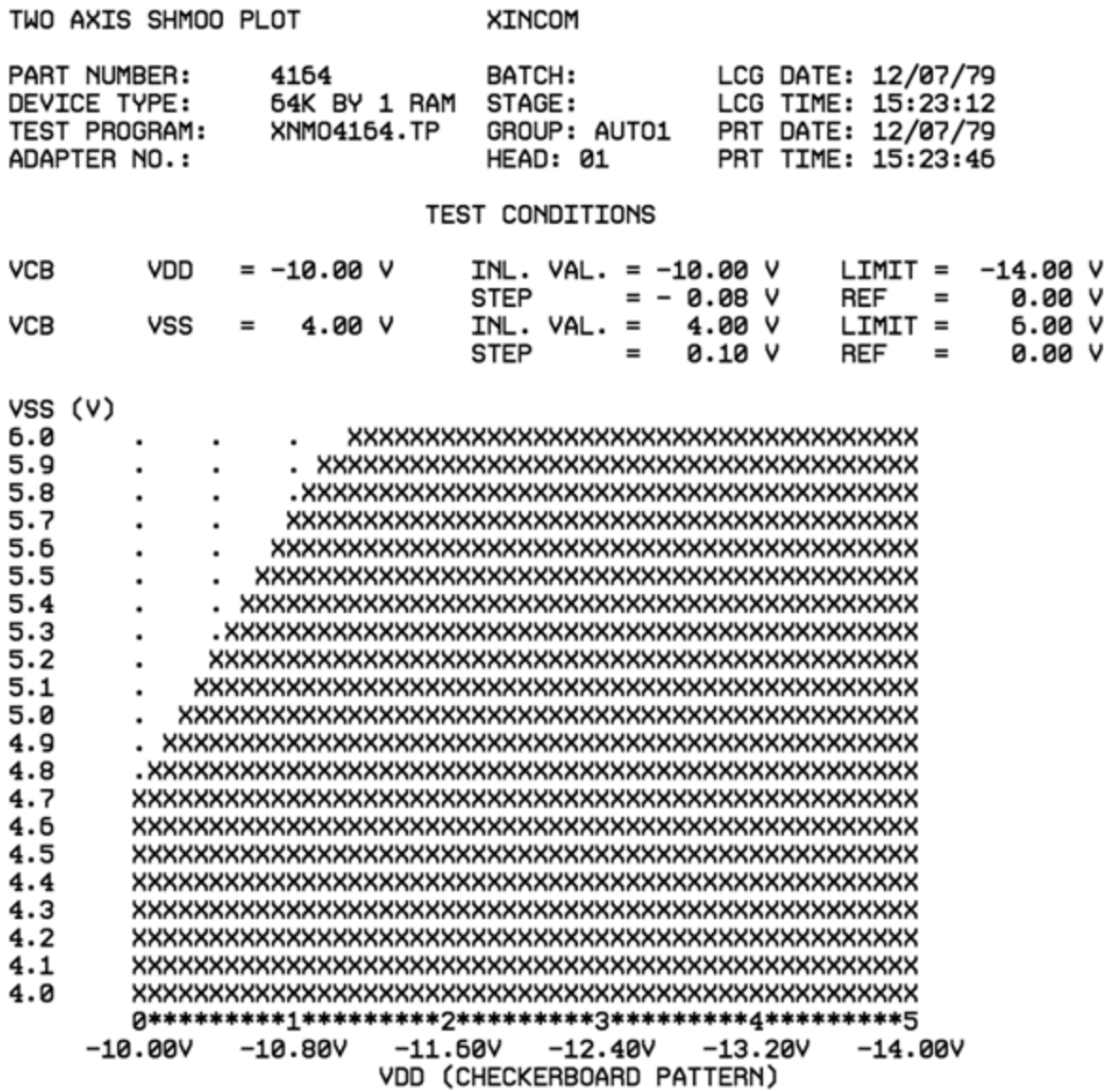
Silicon characterization glossary

- Characterization: testing the design with voltage and frequency shmooing to find the ideal operating conditions
- Shmoo plot: Shows graphically the range of conditions in which DUT operates
- OPP: Operating Performance Point, a list of frequency and voltage pairs



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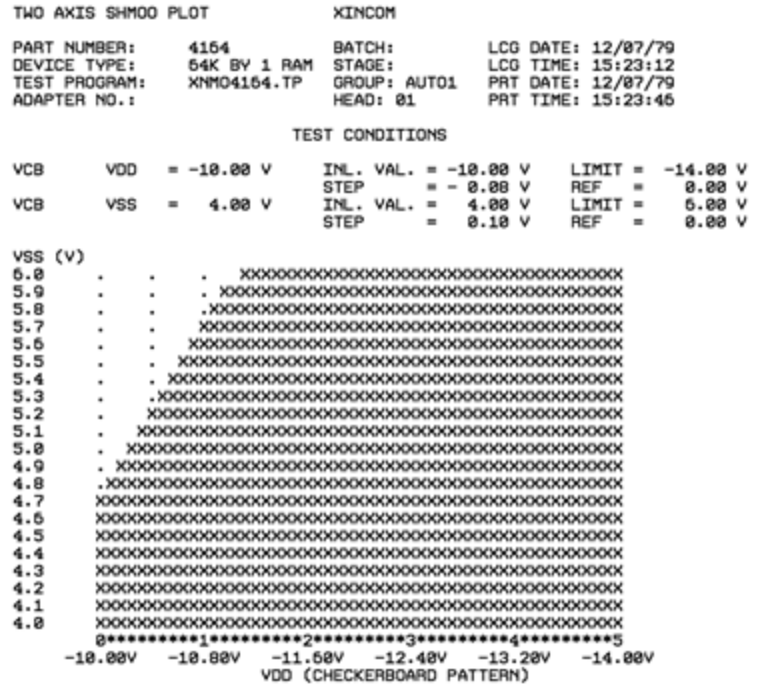
TPMP Alternative developments



- Shmoo machine:
  - Add Voltage control equipment (can be HW or SW)
  - Add Frequency control equipment (SW)

- Automated Power Optimization framework
  - Low power UC optimization goes through an exploration of all the IO configuration + clock gating configuration to achieve ultimate low power optimization
  - This can be achieved automatically by systematic exploration of all the configuration combining TPMP with memtool (sw version or JTAG)

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