Board Bringup: LCD and Display Interfaces

Slides and Resources at

http://www.elinux.org/BoardBringupLCD

Introduction

- Dave Anders aka prpplague

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- Board Bring Up: LCD and Display Interfaces

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- Board Bring Up: LCD and Display Interfaces
  - Challenges of LCD Bring Up

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  - Interface Timings

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  - Challenges of LCD Bring Up
  - Interface Timings
  - Display Interface Types
  - Debugging

Challenges of LCD Bring Up

- Simple User Display

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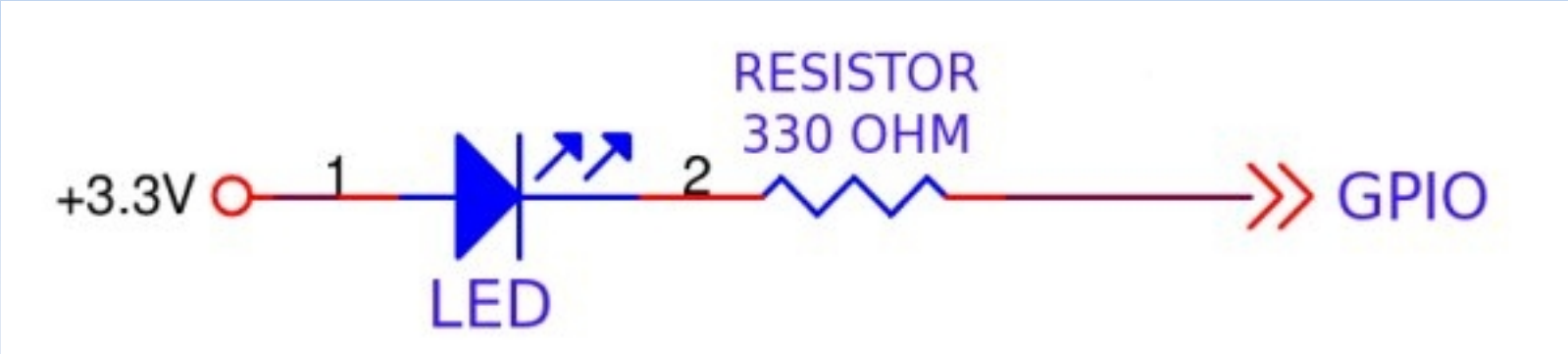
- Simple User Display

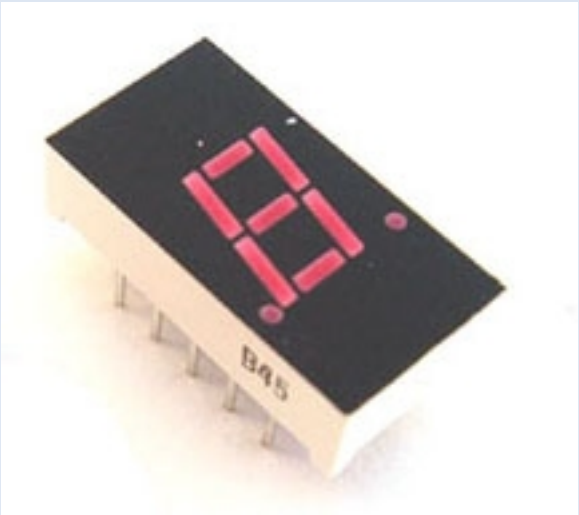


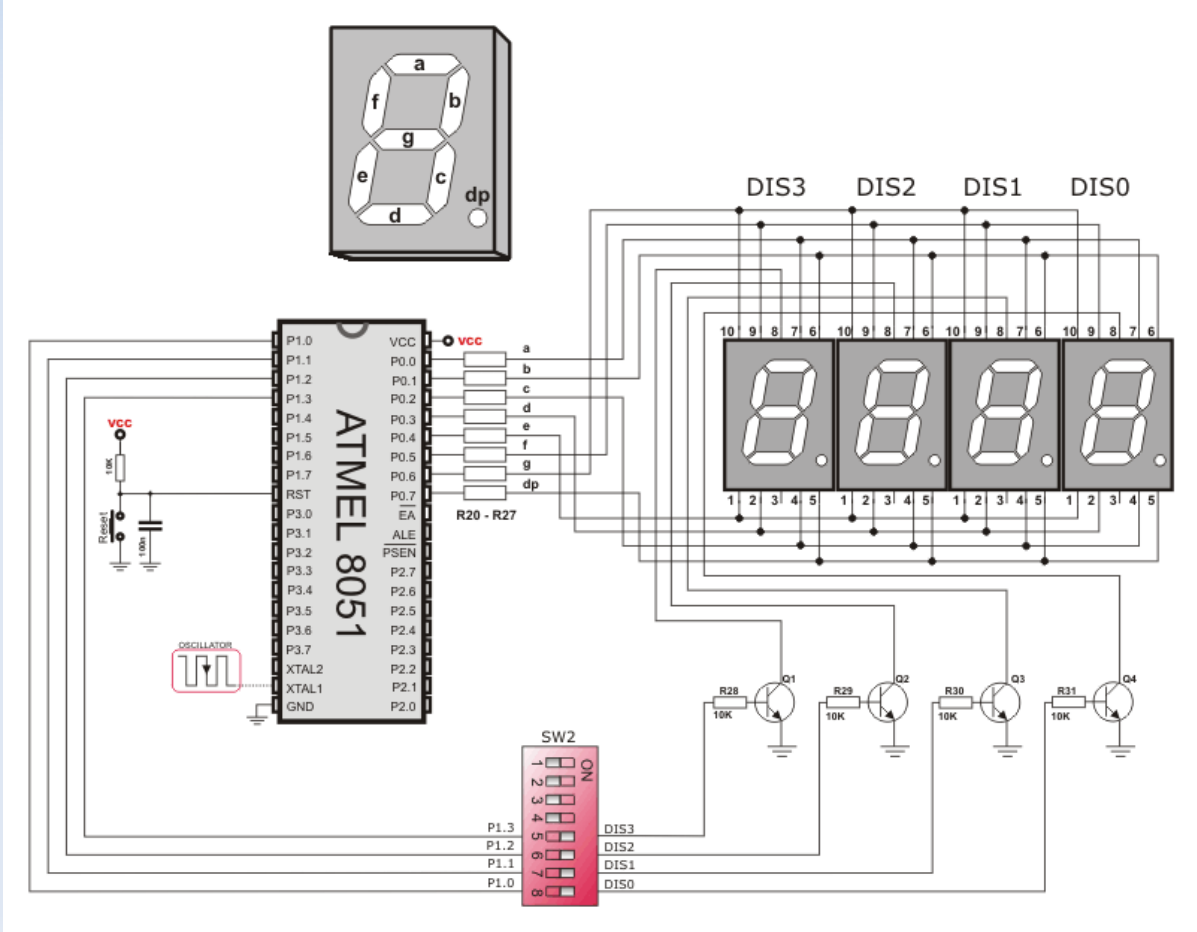
Challenges of LCD Bring Up

- Simple User Display
  - Easy to visualize
  - Easy to measure
  - Easy to program

Challenges of LCD Bring Up

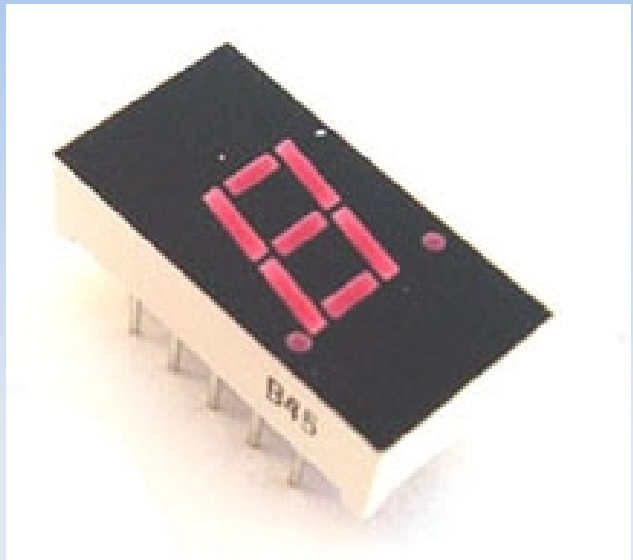
- Simple User Display
- Evolution of Displays





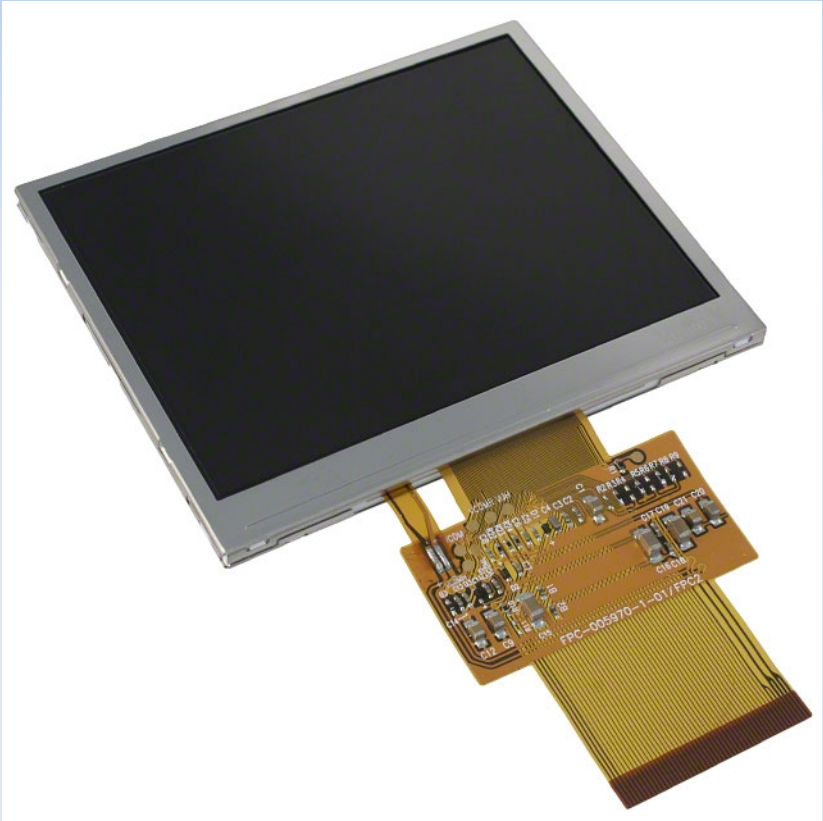
Challenges of LCD Bring Up

- Simple User Display
- Evolution of Displays
  - Clocking
  - Multiple signals
  - Introduction of controllers



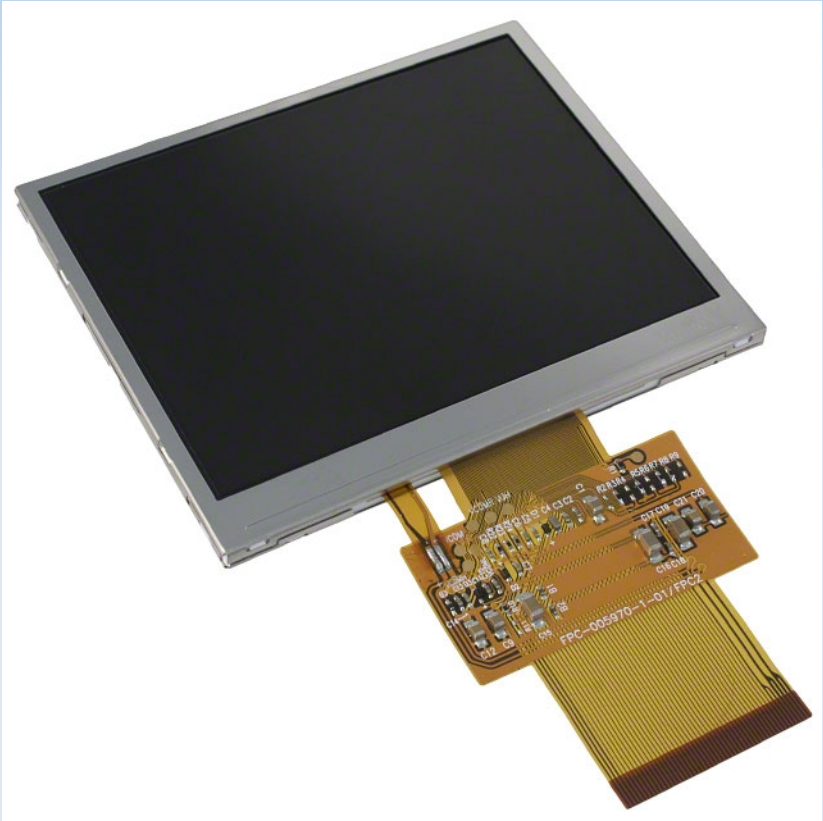
Challenges of LCD Bring Up

- Simple User Display
- Evolution of Displays
- Transition to LCD



Challenges of LCD Bring Up

- Simple User Display
- Evolution of Displays
- Transition to LCD
  - Higher frequency
  - More signals
  - Complex Controllers

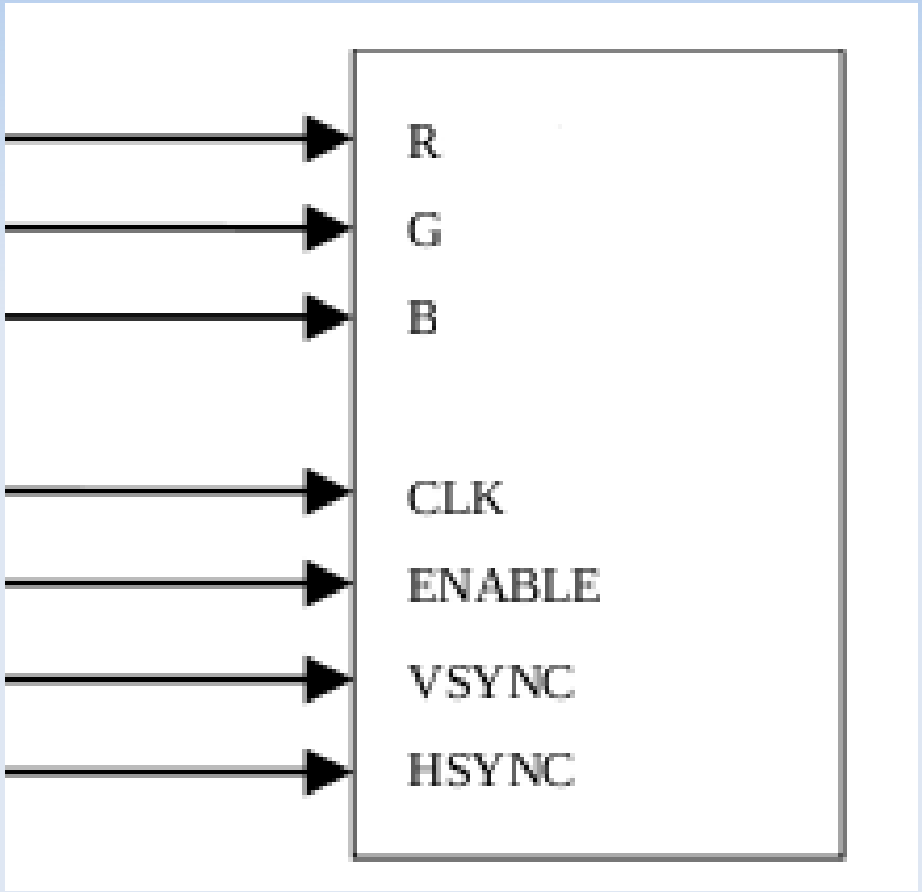


Interface Timings

- TFT Parallel Interface

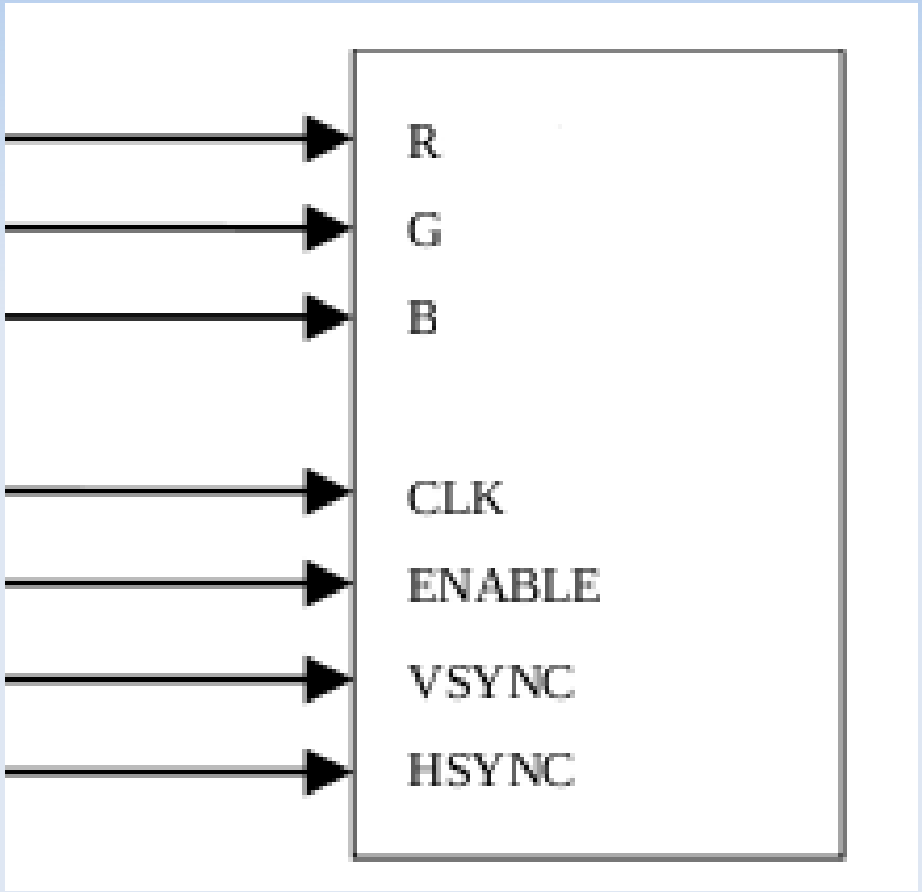
Interface Timings

- TFT Parallel Interface
  - PCLK (Pixel Clock)



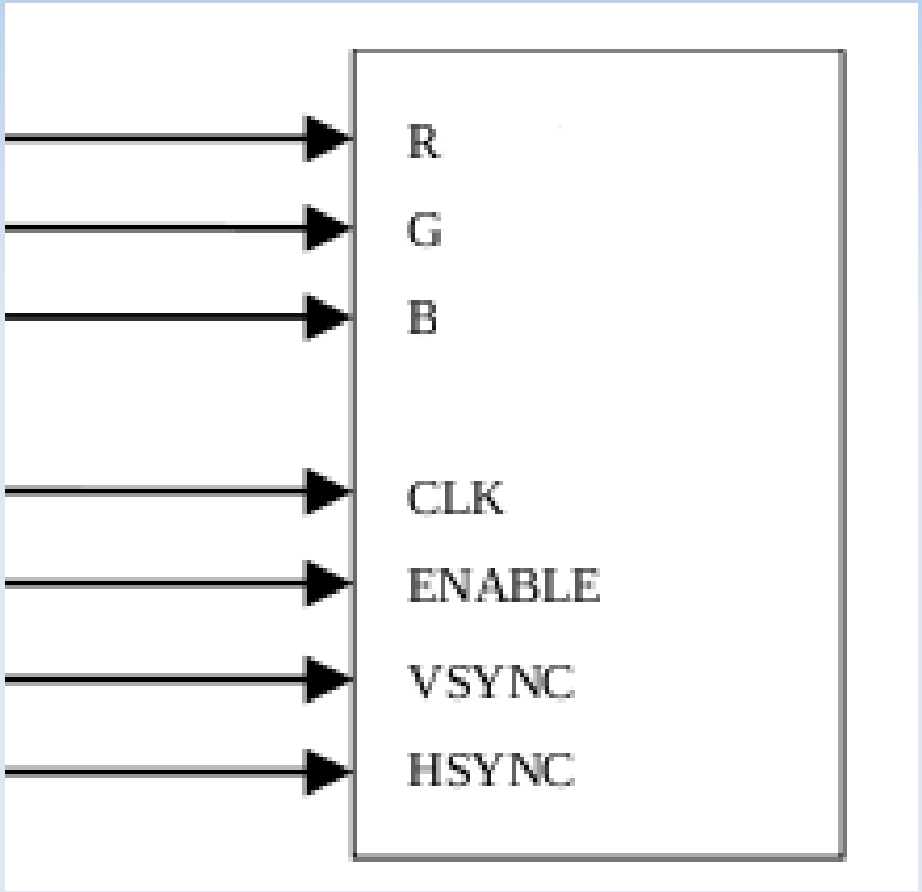
Interface Timings

- TFT Parallel Interface
  - PCLK (Pixel Clock)
  - HSYNC (Horizontal Sync)



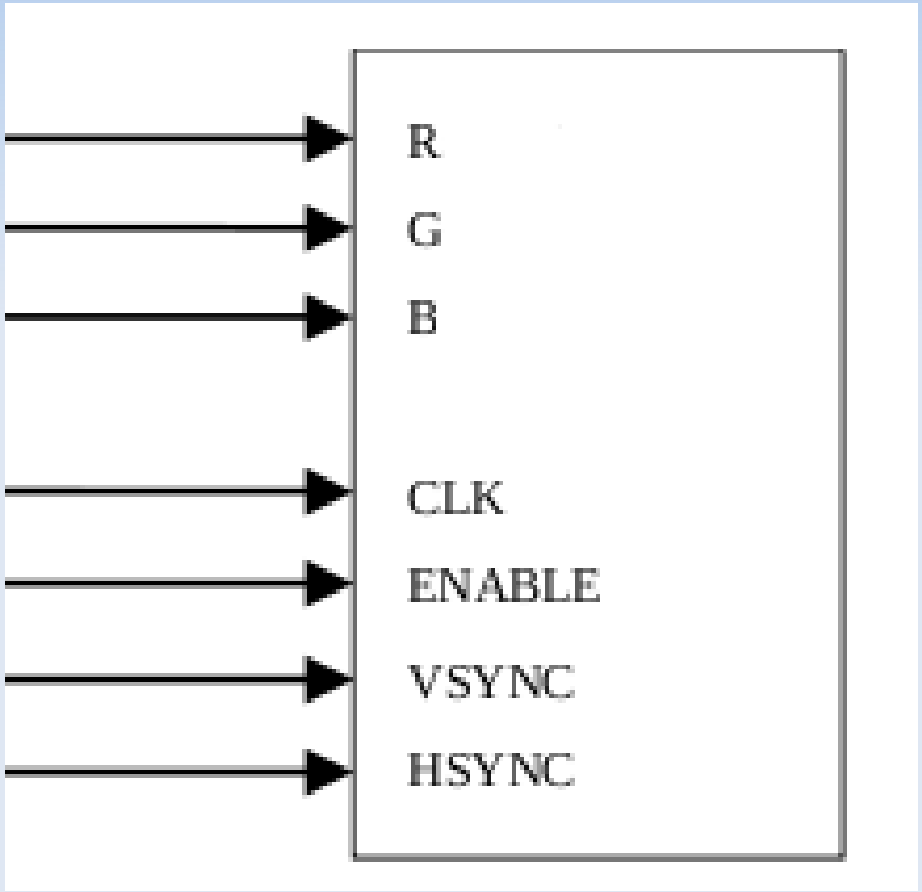
Interface Timings

- TFT Parallel Interface
  - PCLK (Pixel Clock)
  - HSYNC (Horizontal Sync)
  - VSYNC (Verticle Sync)



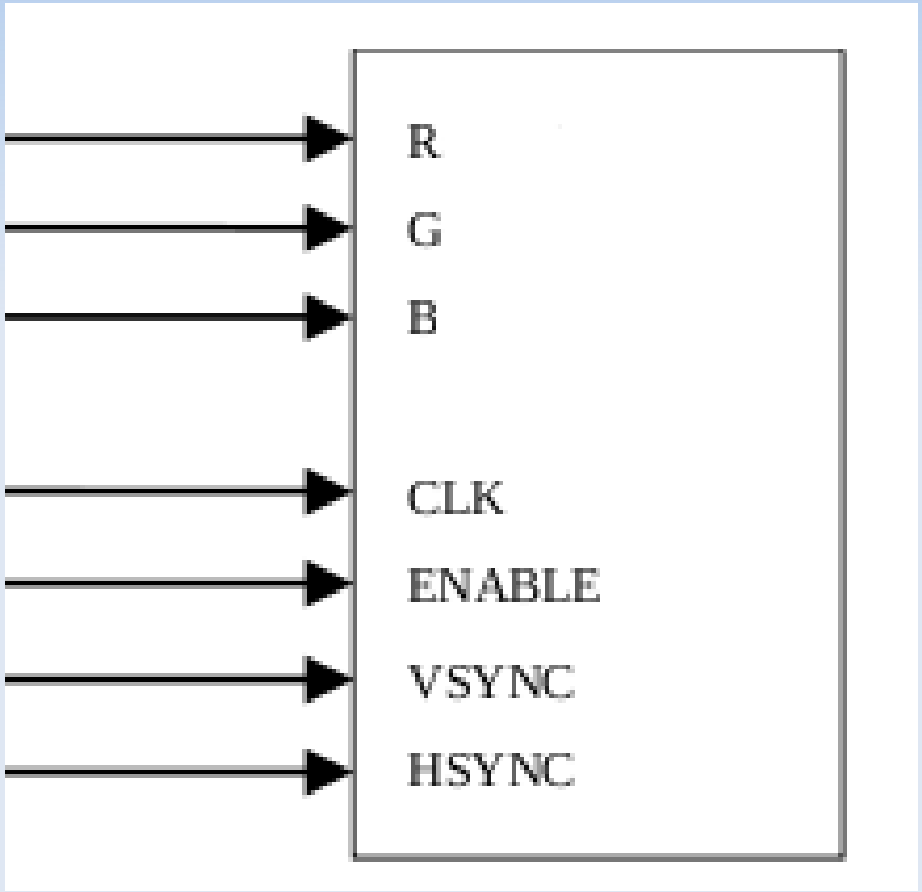
Interface Timings

- TFT Parallel Interface
  - PCLK (Pixel Clock)
  - HSYNC (Horizontal Sync)
  - VSYNC (Verticle Sync)
  - DE (Data Enable)



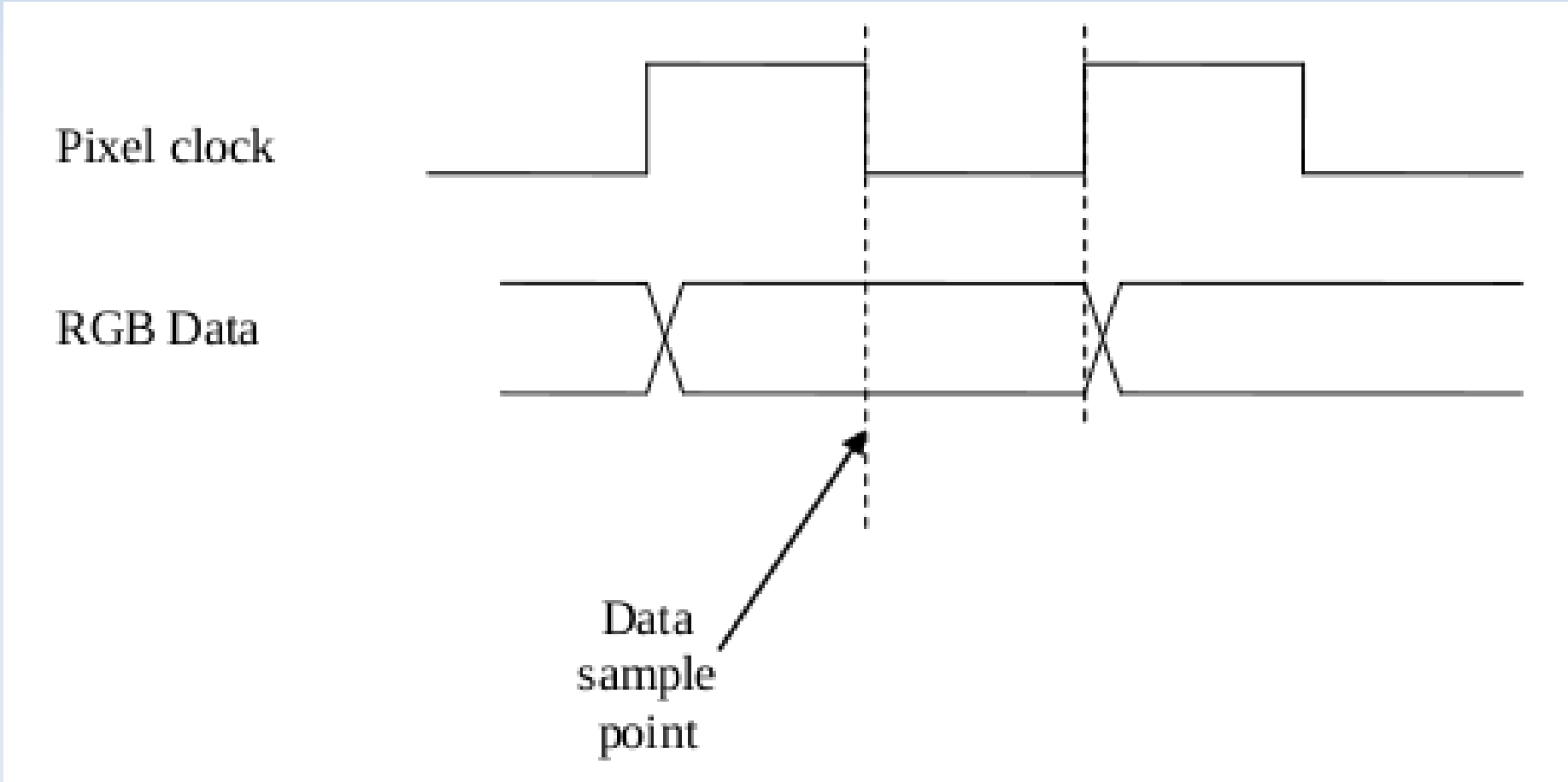
Interface Timings

- TFT Parallel Interface
  - PCLK (Pixel Clock)
  - HSYNC (Horizontal Sync)
  - VSYNC (Verticle Sync)
  - DE (Data Enable)
  - R/G/B (Data Lines)



Interface Timings

- TFT Parallel Interface
- Pixel Clock and RGB Data



Interface Timings

- TFT Parallel Interface
- Pixel Clock and RGB Data
  - 640 Width x 480 Height

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  - Estimated PCLK = 18.432MHz

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- TFT Parallel Interface
- Pixel Clock and RGB Data
  - 640 Width x 480 Height
  - 640 x 480 = 307200 clocks for one frame
  - 307200 x 60 = 18432000 for 60 frames per second
  - Estimated PCLK = 18.432MHz
  - What if your SoC can not create exactly 18.432MHz?

Interface Timings

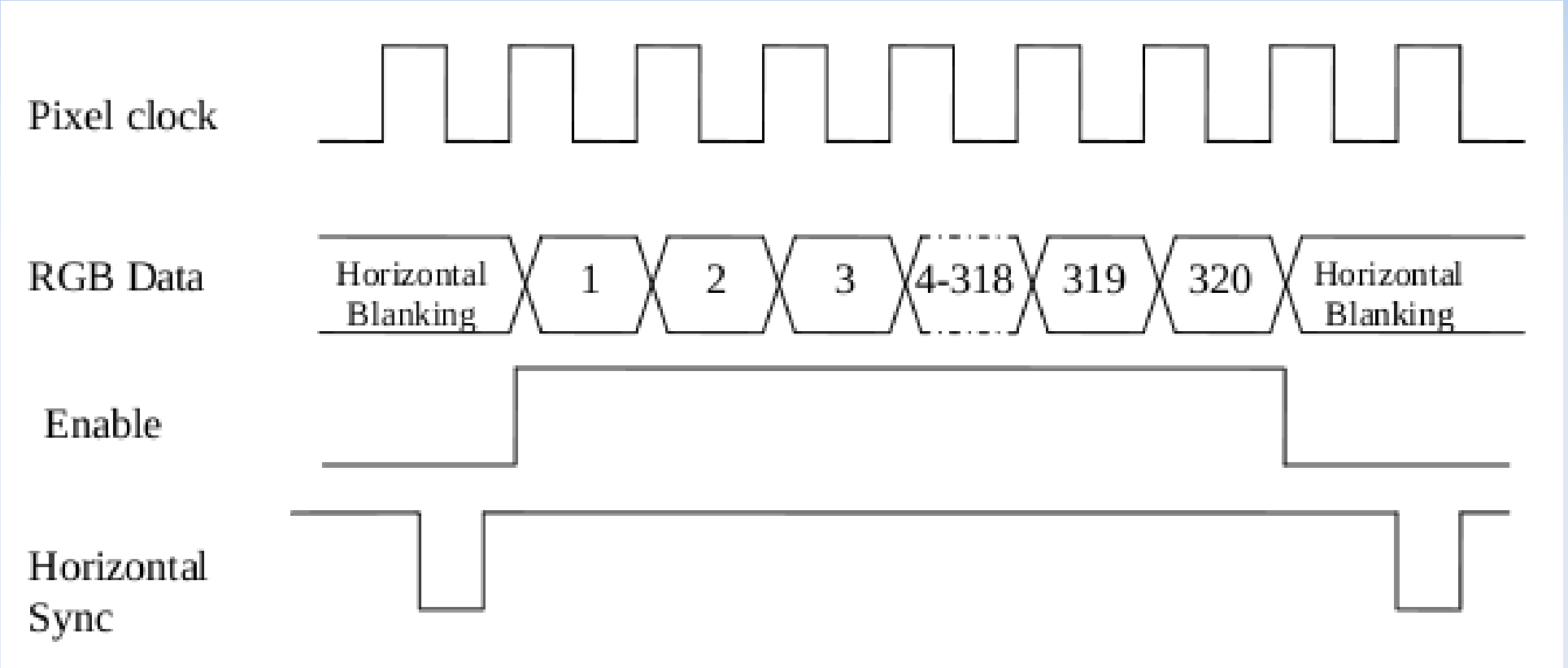
- TFT Parallel Interface
- Pixel Clock and RGB Data
  - 640 Width x 480 Height
  - 640 x 480 = 307200 clocks for one frame
  - 307200 x 60 = 18432000 for 60 frames per second
  - Estimated PCLK = 18.432MHz
  - What if your SoC can not create exactly 18.432MHz?
  - Good question!!!!!

Interface Timings

- TFT Parallel Interface
- Pixel Clock and RGB Data
- Line Timing – HSYNC and DE

Interface Timings

Horizontal SYNC and Data Enable



Interface Timings

- TFT Parallel Interface
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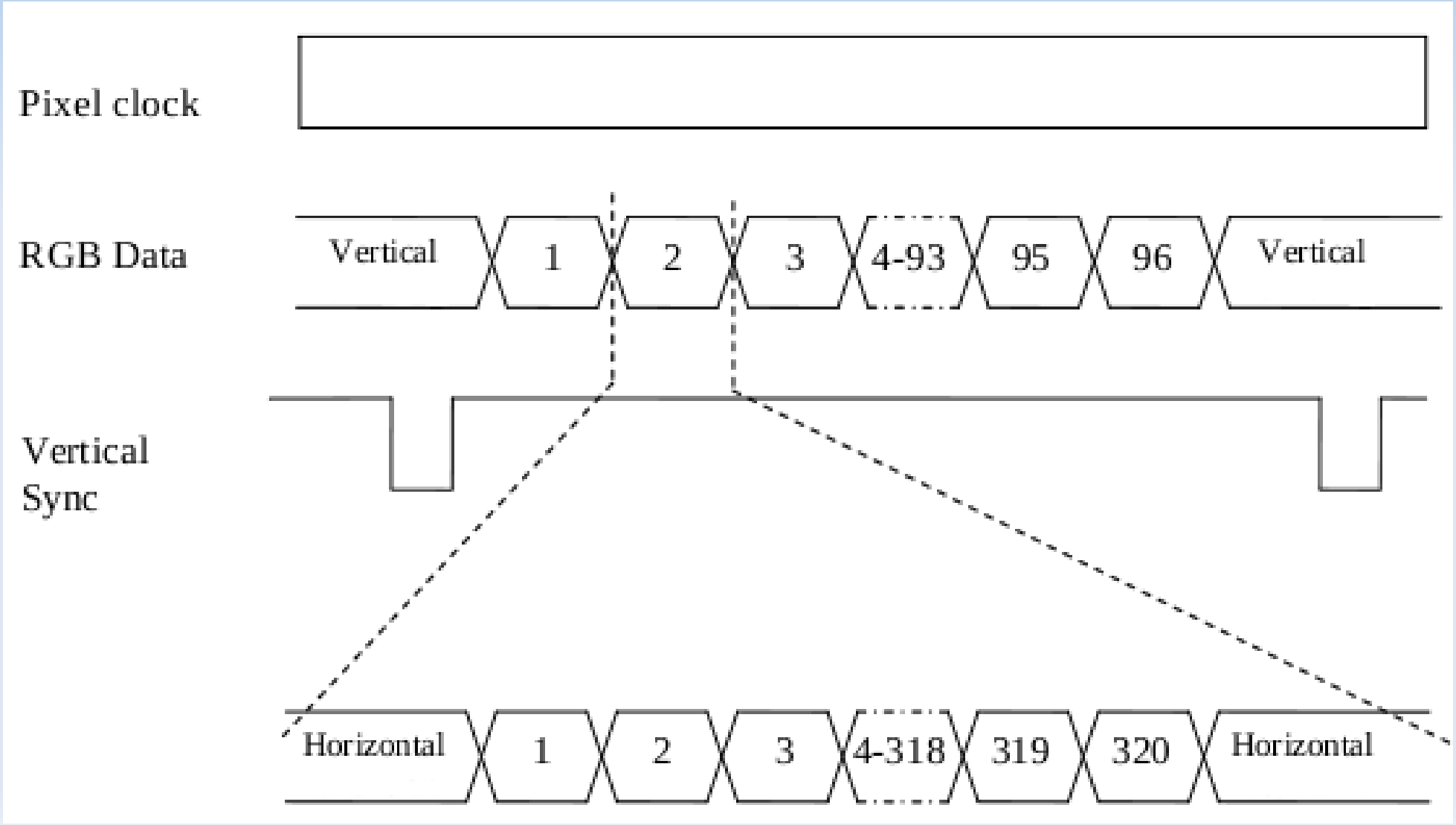
- Line Timing – HSYNC and DE
- Frame Timing - VSYNC

Interface Timings

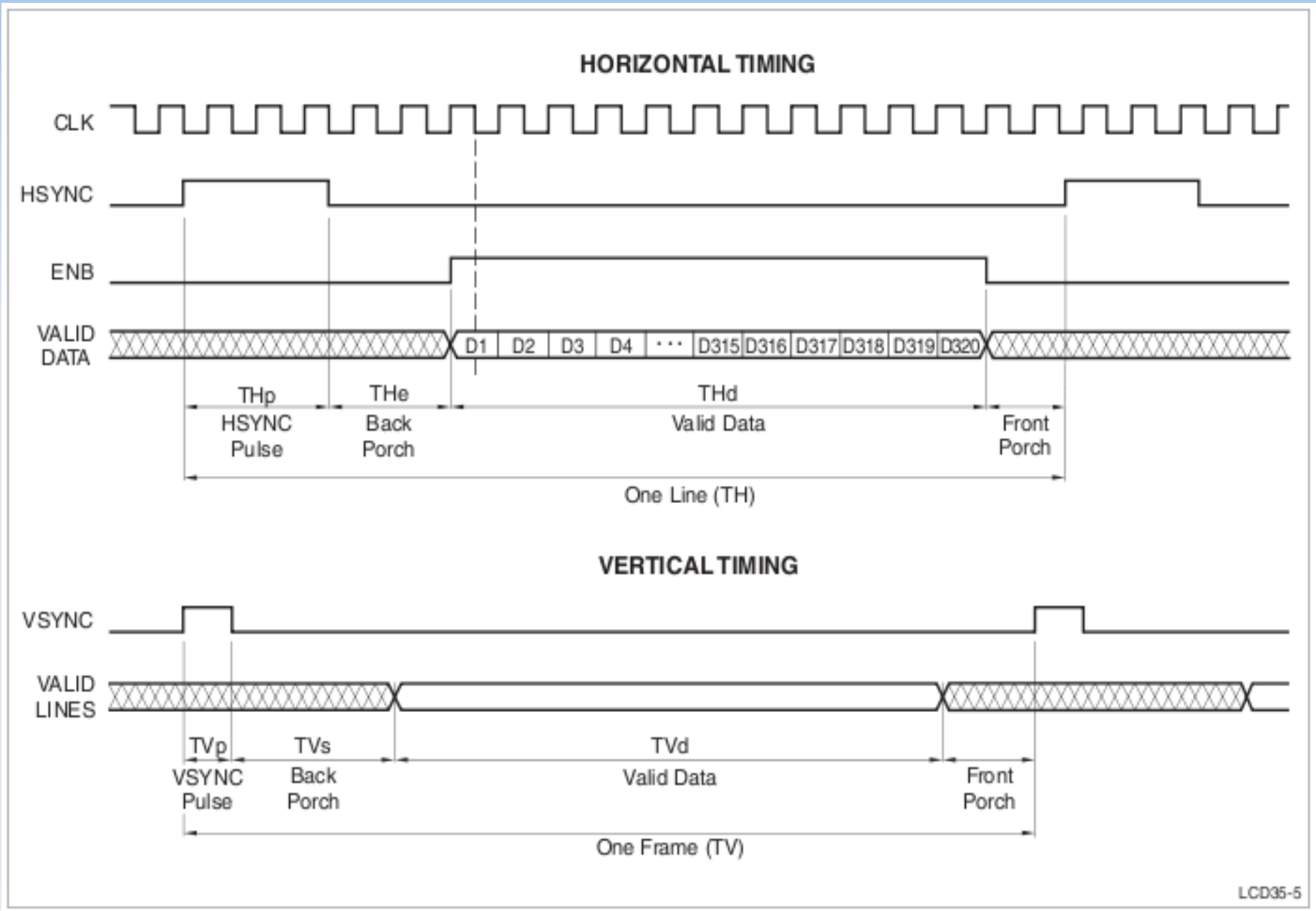
Vertical SYNC



Interface Timings

- TFT Parallel Interface
- Pixel Clock and RGB Data
- Line Timing – HSYNC and DE
- Frame Timing – VSYNC
- Front Porch / Back Porch / Sync Width
  - Remember the question about exact pixel clock?

Interface Timings



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  - Remember the question about exact pixel clock?
  - Values in the datasheet

Interface Timings

- TFT Parallel Interface
- Pixel Clock and RGB Data
- Line Timing – HSYNC and DE
- Frame Timing – VSYNC
- Front Porch / Back Porch / Sync Width
  - Remember the question about exact pixel clock?
  - Values in the datasheet
  - Lots of numbers to keep track of

Display Interface Types

- Disadvantages of Parallel Interface

Display Interface Types

- Disadvantages of Parallel Interface
  - Large Number of Signals
  - Limited Distance
  - Lack of Standardization

Display Interface Types

- Disadvantages of Parallel Interface
- Differential Interfaces

Display Interface Types

- Disadvantages of Parallel Interface
- Differential Interfaces
  - Reduced number of signals
  - Longer distances
  - Standardized

Display Interface Types

- Disadvantages of Parallel Interface
- Differential Interfaces
- Common Differential Interfaces

Display Interface Types

- Disadvantages of Parallel Interface
- Differential Interfaces
- Common Differential Interfaces
  - LVDS – Low Voltage Differential Signaling

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  - DVI - Digital Visual Interface

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  - DVI - Digital Visual Interface
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Display Interface Types

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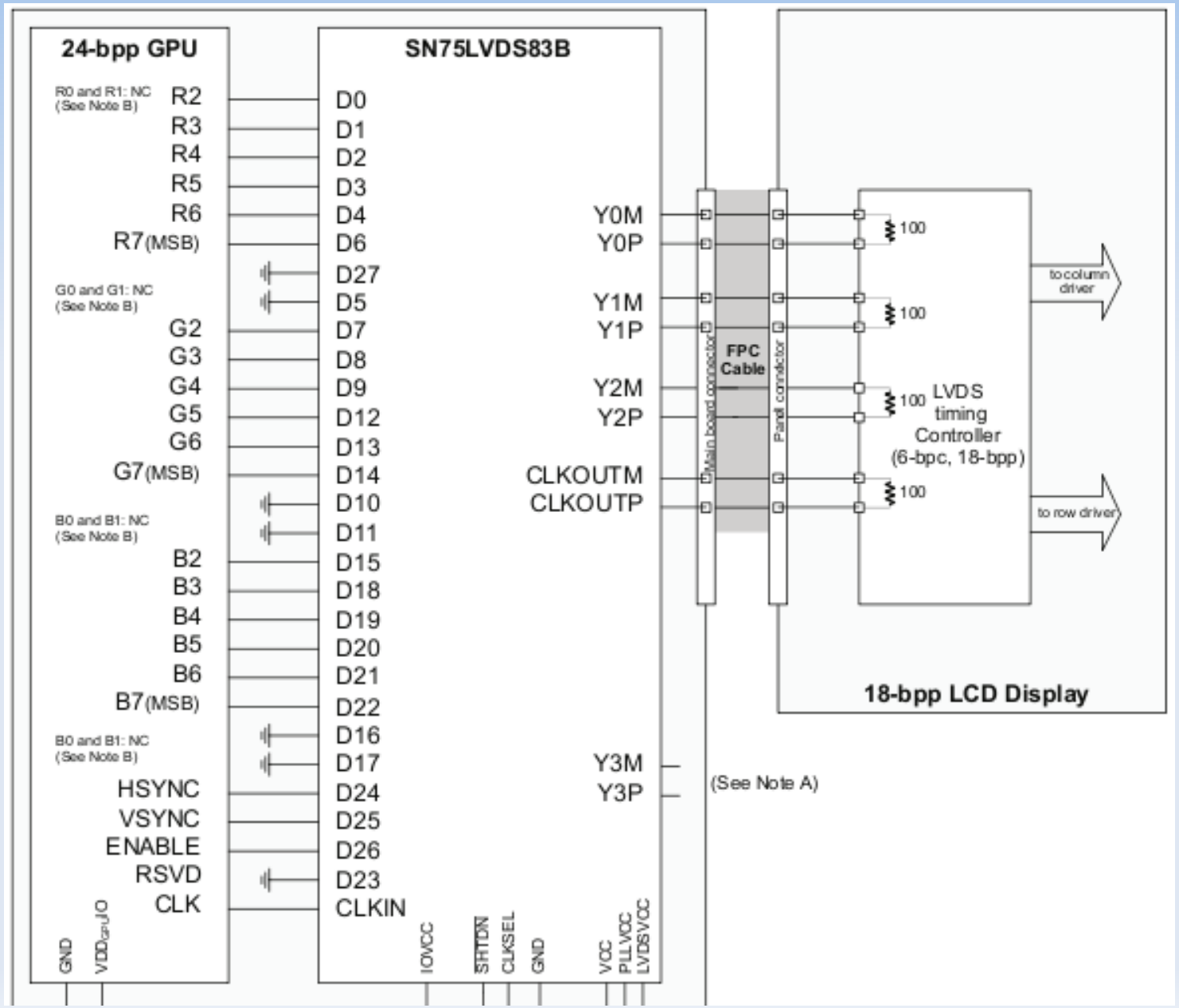
- Common Differential Interfaces
  - LVDS – Low Voltage Differential Signaling
  - DVI - Digital Visual Interface
  - HDMI - High-Definition Multimedia Interface
  - DisplayPort

Display Interface Types

- Disadvantages of Parallel Interface
- Differential Interfaces
- Common Differential Interfaces
- Why learn TFT when working with Differential?

Display Interface Types



Display Interface Types

- Disadvantages of Parallel Interface
- Differential Interfaces
- Common Differential Interfaces
- Why learn TFT when working with Differential?
  - LVDS SN75LVDS83B – SN75LVDS82
  - DVI TFP410 – TFP401

Display Interface Types

- Disadvantages of Parallel Interface
- Differential Interfaces
- Common Differential Interfaces
- Why learn TFT when working with Differential?
- Combination Interfaces

Display Interface Types

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- Why learn TFT when working with Differential?
- Combination Interfaces
- EDID
  - Extended Display Identification Data
  - Contents

Display Interface Types

- EDID Contents
  - Multiple Configurations
  - Pixel Clock Frequency
  - Resolution
  - Color Depth
  - Front Porch / Back Porch
  - SYNC width

Display Interface Types

- Disadvantages of Parallel Interface
- Differential Interfaces
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- Why learn TFT when working with Differential?
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  - I2C EEPROM at 0x50

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  - parse-edid

Debugging

- Logic Analyzer
  - Importance of visualization

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  - Open source (or open source friendly)

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- Logic Analyzer
  - Importance of visualization
  - Pixel clock frequency
  - Open source (or open source friendly)
    - SIGROK
    - ChronoVu LA8 (less than $200)

Debugging

- Logic Analyzer
- Reference Platform
  - Same platform – different display
  - Different platform – same display
  - Compatible display
  - Kernel sources

Debugging

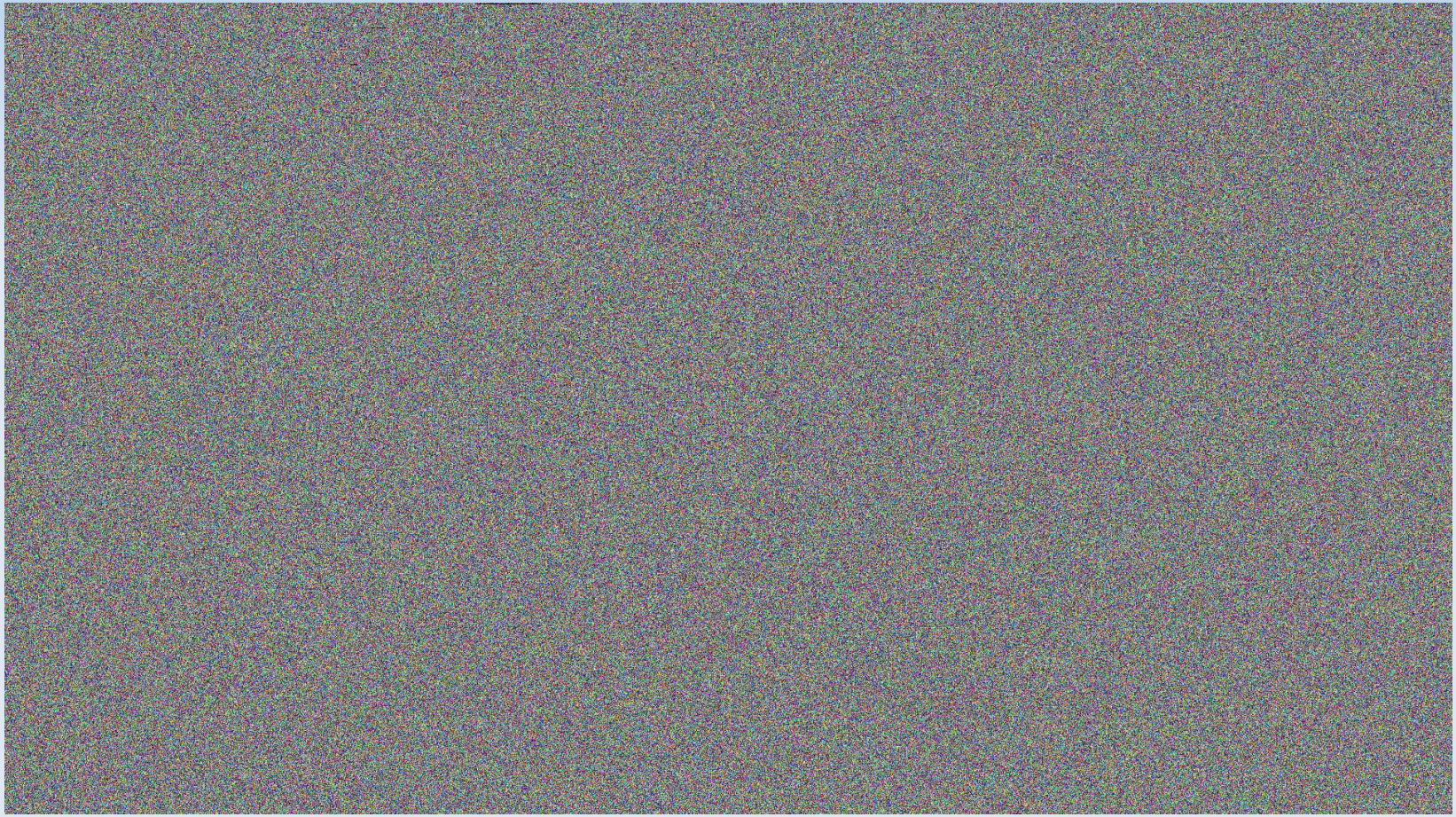
- Logic Analyzer
- Reference Platform
- Display Simulation
  - Lower resolution
  - Transmitter Chips TFP410 to DVI display
  - Receive Chips LVDS to SN75LVDS82

Debugging

- Logic Analyzer
- Reference Platform
- Display Simulation
- Userspace debugging

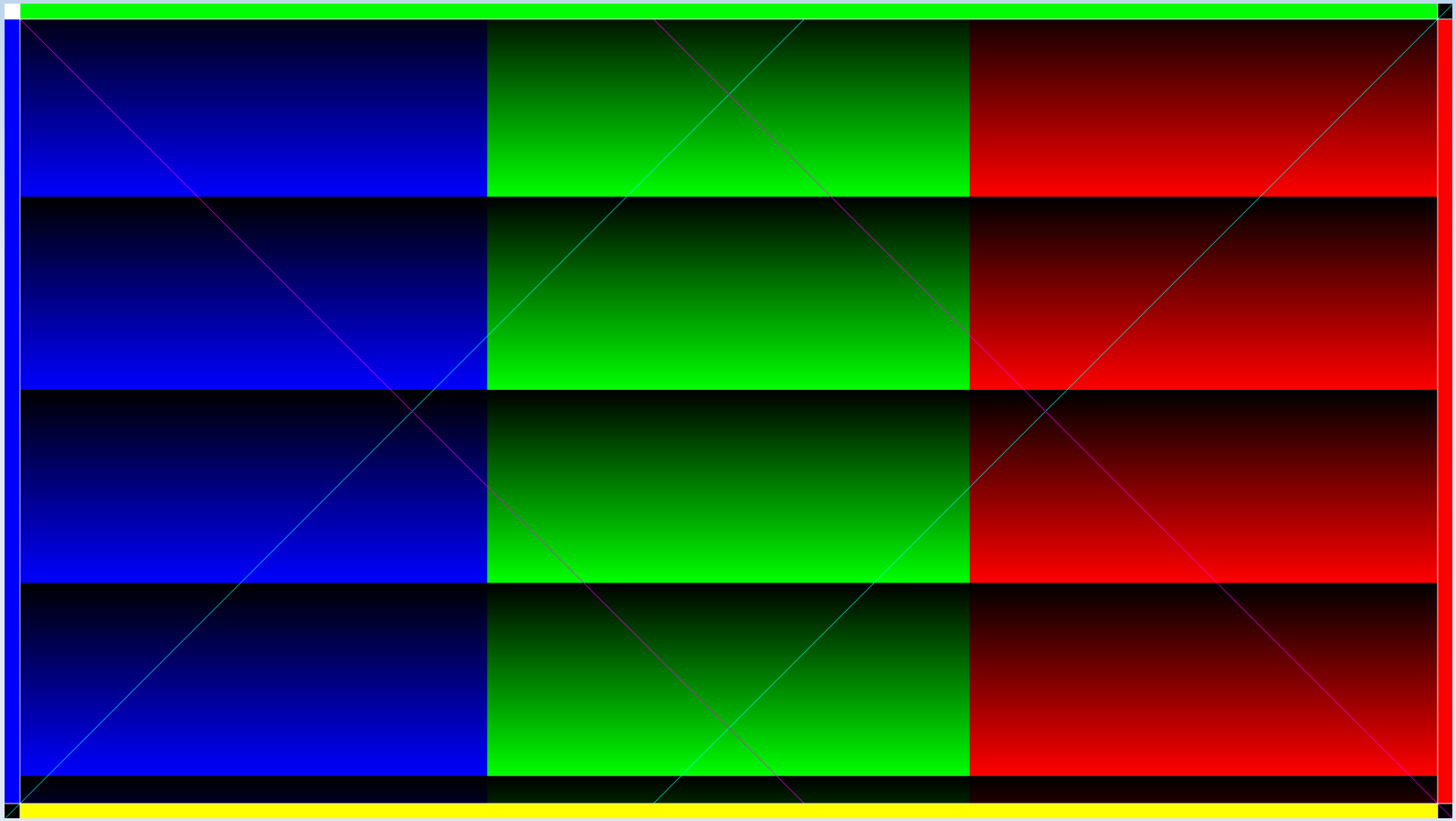
Debugging

- cat /dev/urandom > /dev/fb0



Debugging

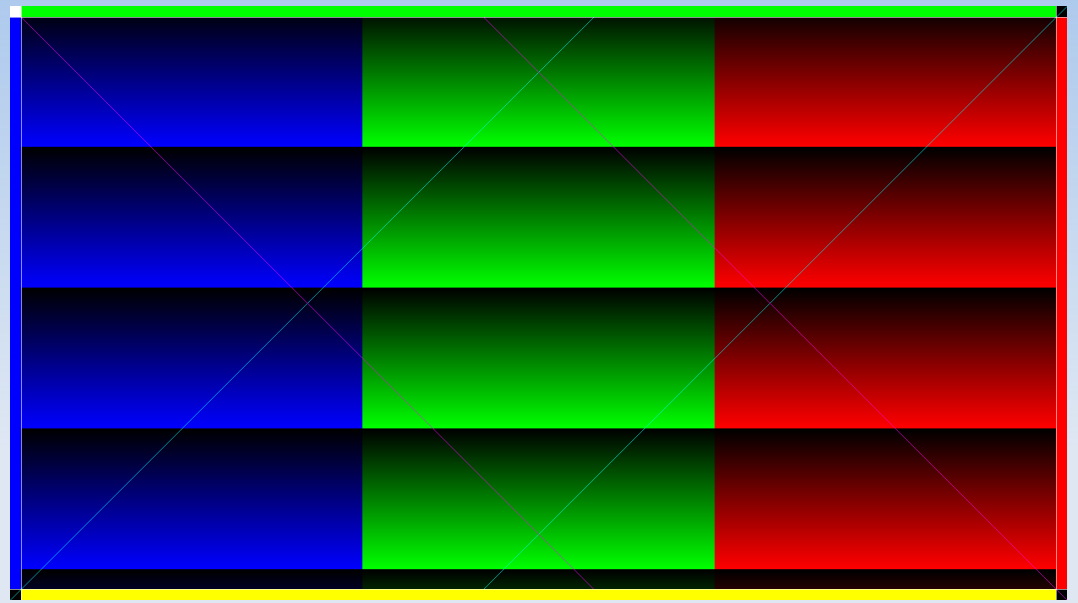
- fb-test

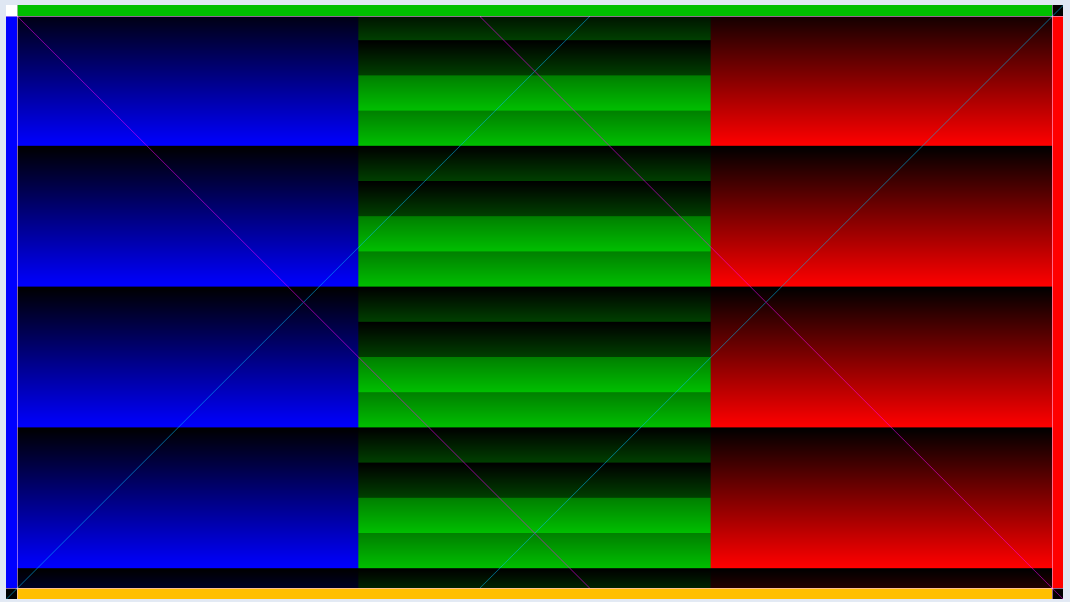


Debugging

Missing Green

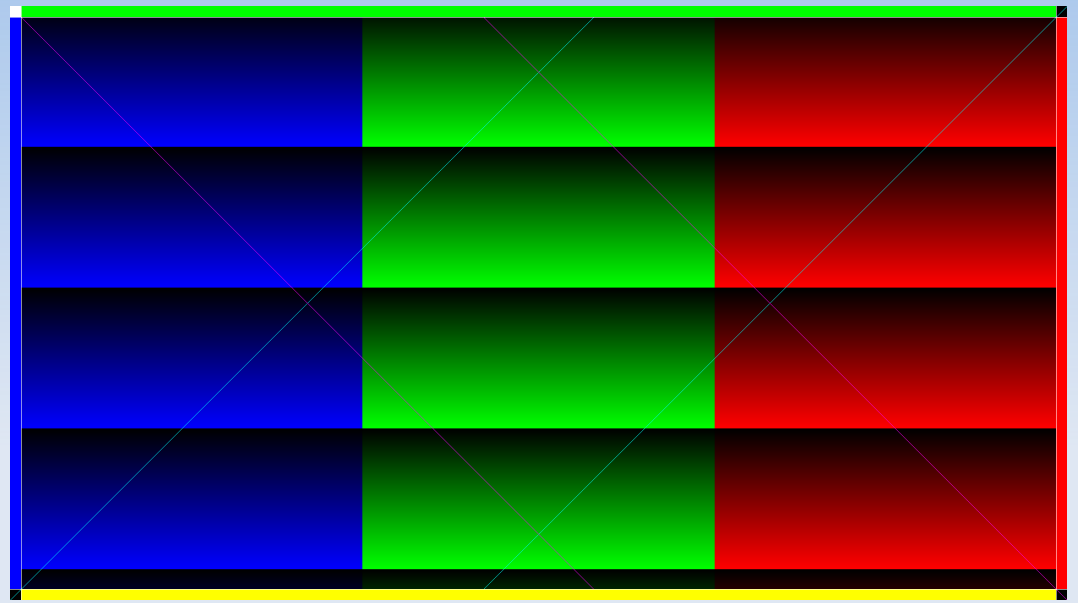
Data Bit

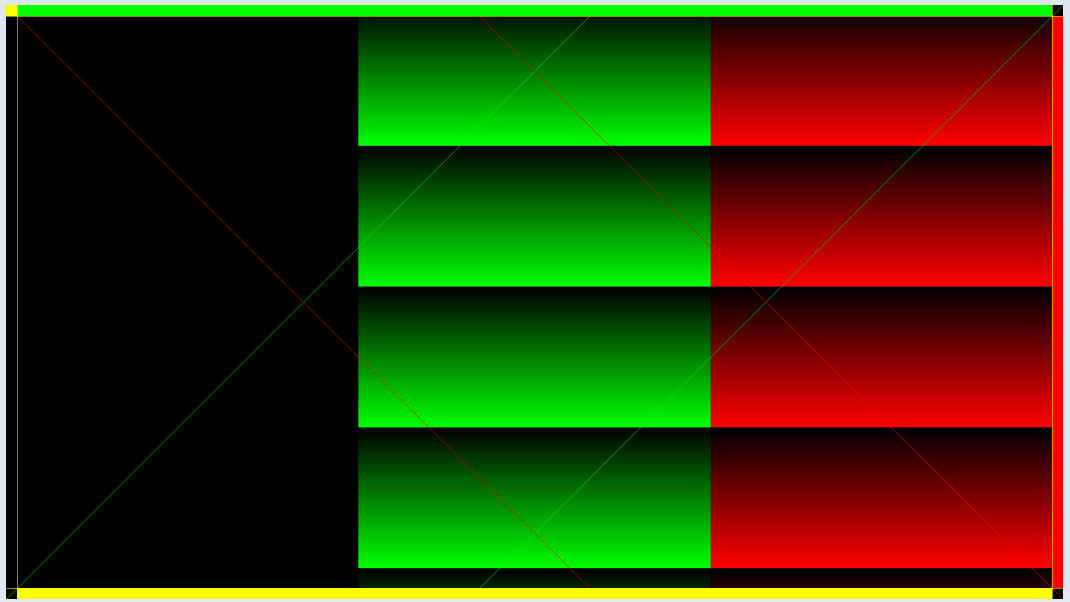




Debugging

Missing Blue Signals

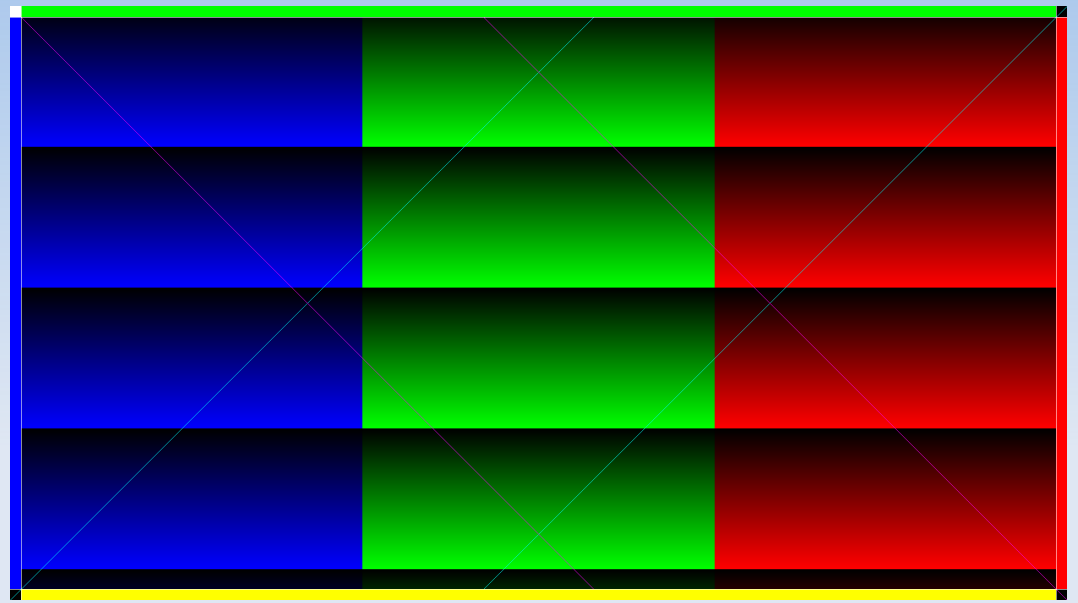


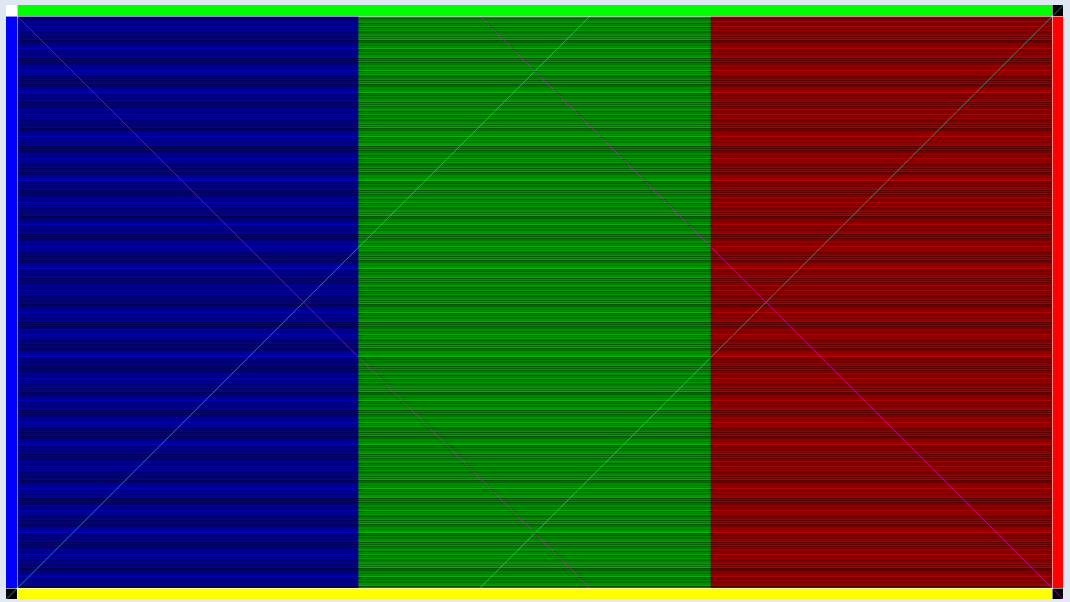


Debugging

LSB/MSB

Signal Swap

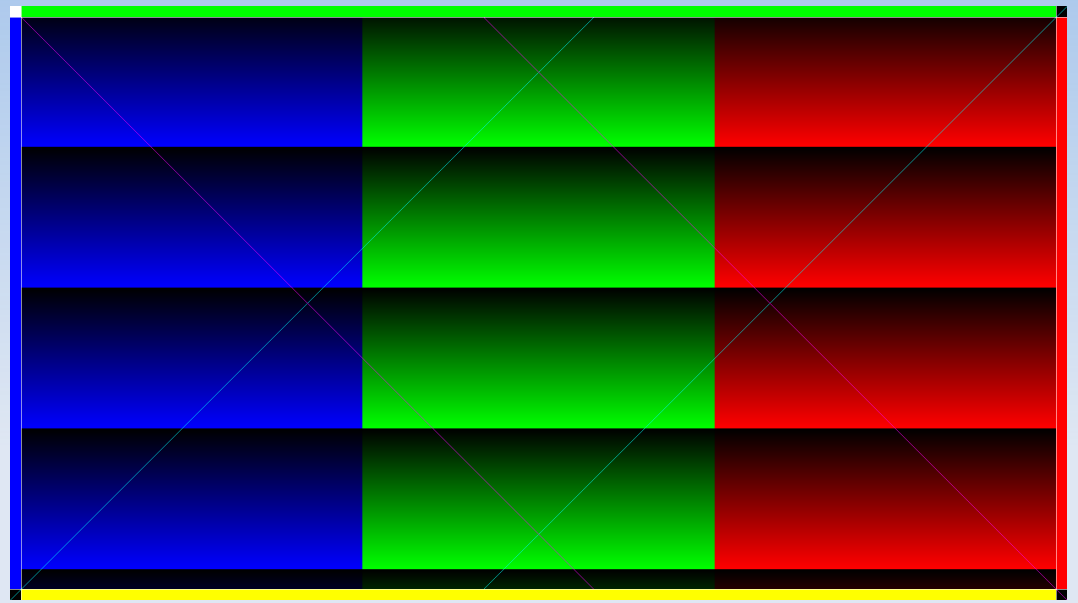


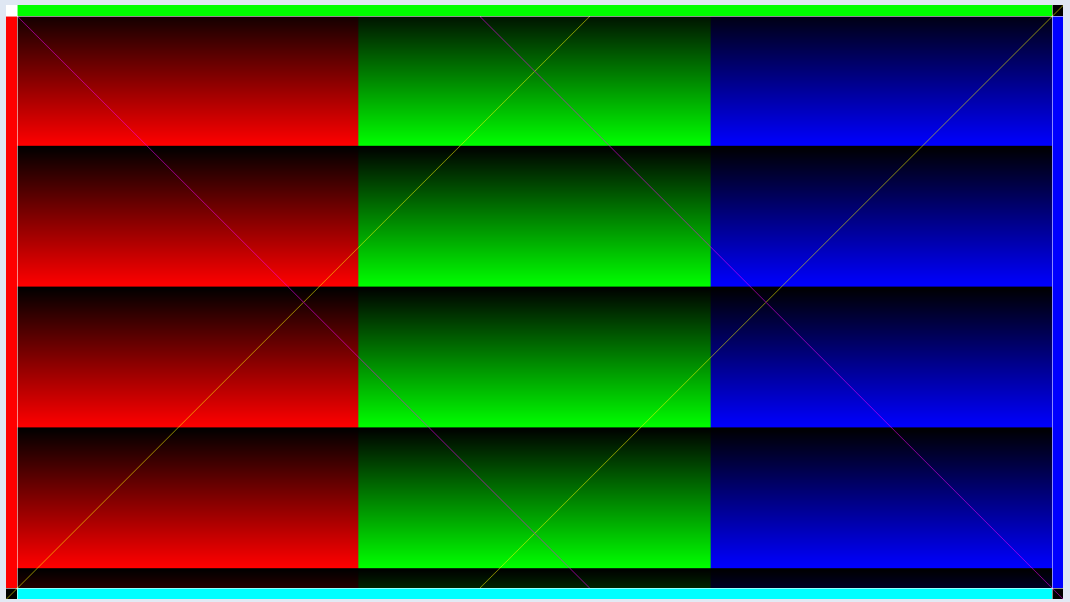


Debugging

Red/Blue

Signal Swap





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  - Challenges of LCD bring up
  - Interface Timings
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Questions?