RZ/G1M Starter Kit
Board Hardware Manual

YR8A77430HA02BG
(Platform version device)

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# Revision History

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<td>First revision issued.</td>
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1. Overview

The RZ/G1M is a new generation product featuring the functionality required for the Human Machine Interface systems. Its newly employed bus configuration maximizes system performance, space saving, and cost efficiency.

The RZ/G1M Starter Kit Board, is an RZ/G1M-specific evaluation board that can be used to evaluate solutions using the RZ/G1M and to develop operating systems, device drivers, and applications. Using the RZ/G1M Starter Kit Board allows the developers to efficiently conduct required tasks such as evaluation of the RZ/G1M system performance and thus greatly reduces the turn-around time in product development.

1.1. Features

1.1.1. The RZ/G1M includes:

- Two 1.5-GHz ARM Cortex™-A15 MCore™ cores (dual core: option)
- Memory controller for DDR3-SDRAM (DDR3-1600) with 32 bits × 2 channel
- Three-dimensional graphics engines
- Video processing unit
- Sound processing unit
- SD card host interface (3 channels), MMCIF (1 channel)
- USB2.0 host (1 channel), USB2.0 host/function (1 channel)
- DU (digital RGB 2 channels), DCU, TCON, VIN (2 channels)
- VSP1, VCP3, FDP1, 2D-DMAC
- SCU, SSIU (10 channels), ADG
- CAN, Ethernet MAC, Ethernet AVB
- WDT, TPU, CMT1, TMU, CPG, INTC, DAC, LBSC
- I²C (5 channels), IIC (2 channels), SCIF (6 channels), SCIFA (6 channels), SCIFB (3 channels), MSIOF (3 channels), QSPI, HSCIF (3 channels), PWM (7 channels)
- GPIO, etc
- Power supply voltages (typ.) 3.3 V, 1.8 V, 1.5 V/1.35 V, 1.0 V
## 1.1.2. The RZ/G1M Starter Kit Board includes:

### Table 1.1.1 List of RZ/G1M Starter Kit Board Functions (1)

<table>
<thead>
<tr>
<th>Board Function</th>
<th>Module</th>
<th>Description</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>RAM</strong></td>
<td>DDR3</td>
<td>Dual Channel DDR3L-1600. 1Gbyte x2 channels, 32bit data width x2 channels. 4Gbit (16bit data width) x4 devices. SDRAM Backup feature: Not Supported.</td>
<td>Pin Multi: HY57F14G620AF-6C8 x4</td>
</tr>
<tr>
<td><strong>ROM</strong></td>
<td>LBSC</td>
<td>No device.</td>
<td>Pin Multi: QSPI</td>
</tr>
<tr>
<td><strong>Debug I/F</strong></td>
<td>DBG</td>
<td>Connector: HTST-110-01-S-DV (20pin)</td>
<td>Related Jumper: JP2</td>
</tr>
<tr>
<td><strong>SCI0</strong></td>
<td>USB2.0 I/F</td>
<td>USB2.0 Host or Function</td>
<td>Pin Multi: SAT_1A</td>
</tr>
<tr>
<td><strong>SCI1</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>LAN</strong></td>
<td>EtherMAC</td>
<td>Debug Ether(100Mbp)</td>
<td>For Interrupt: RJ0</td>
</tr>
<tr>
<td><strong>SATA 1F</strong></td>
<td>SATA0</td>
<td>Connector: CN4: HSAT-M07-VSD-40</td>
<td>Pin Multi: USB3.0</td>
</tr>
<tr>
<td><strong>PCIE 1F</strong></td>
<td>PCl express</td>
<td>PCI Express Base Specification Revision 2.0, 1-lane, 2.5GT/s or 5.0GT/s</td>
<td>Pin Multi: SAT_1A</td>
</tr>
<tr>
<td><strong>USB2.0 1F</strong></td>
<td>USB2.0 ch0</td>
<td>USB2.0 Host or Function</td>
<td>Connector: Type miniAB.</td>
</tr>
<tr>
<td><strong>USB2.0 ch1</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>SATA I/F</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>SDHI</strong></td>
<td>SDH0</td>
<td>Connector: SD Card slot. Interface voltage: Either 3.3V or 1.8V.</td>
<td>For voltage control: GP2_12</td>
</tr>
<tr>
<td><strong>SDHI</strong></td>
<td>SDH1</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>SDHI</strong></td>
<td>SDH2</td>
<td>Connector: microSD Card slot. DBG3 can be connected instead of microSD card. Interface voltage: Either 3.3V or 1.8V.</td>
<td>For voltage control: GP2_26</td>
</tr>
<tr>
<td><strong>Video Output</strong></td>
<td><strong>DUO_LVDS</strong></td>
<td>LVDS output. 5 pair (CLK, CH0~CH3)</td>
<td>For Interrupt: RJ0</td>
</tr>
<tr>
<td><strong>Video Input</strong></td>
<td><strong>VIN0</strong></td>
<td>TCBG Blit. B1666. Video Decoder: Analog Devices ADV7180WBSCP322. Connector: CN15 RCA</td>
<td>For Interrupt:</td>
</tr>
<tr>
<td>**               **</td>
<td><strong>VIN1</strong></td>
<td>Connector: EXD Connector B (CN3 : G930-030-01-L-D-A-K)</td>
<td>Pin Multi: EtherAVB</td>
</tr>
<tr>
<td>Board Function</td>
<td>Module</td>
<td>Description</td>
<td>Note</td>
</tr>
<tr>
<td>----------------</td>
<td>--------</td>
<td>-------------</td>
<td>------</td>
</tr>
<tr>
<td>Audio</td>
<td>SS0, SS1</td>
<td>Either [A] or [B]</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SS2, SS3</td>
<td>[A] Audio Output (SS0, SS1)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>[A] Audio Jack x1 for stereo line output</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>[A] Audio Multi-Channel Output (SS0, SS1, SS2, SS3)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>HDMI Transmitter AV17911W8002WZ</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Connector: HDMI standard type A</td>
<td>Related Jumper: JF3</td>
</tr>
<tr>
<td></td>
<td>SS0, SS14</td>
<td>EX0 Connector A (CN23: QSE-000-01F-D-A)</td>
<td>Connect to CN23 as GP102_0, 16, 11, 14</td>
</tr>
<tr>
<td></td>
<td>SS2, SS3</td>
<td>EX0 Connector A (CN23: QSE-000-01F-D-A)</td>
<td>Connect to CN23 as GP102_15, 16, 17, 18</td>
</tr>
<tr>
<td>CAN</td>
<td>RCAN</td>
<td>ON111_JW-HS002S-02-H</td>
<td>CAN interface: Maxim MA3351 (3.3V)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>This interface is connected to the following devices</td>
<td>Related Jumper: JF4</td>
</tr>
<tr>
<td>POEF</td>
<td>FC1</td>
<td>Interface voltage: 3.3V</td>
<td>This interface is connected to the following devices: PMIC DA9803 (AlternateHSD-2C)</td>
</tr>
<tr>
<td></td>
<td>FC2</td>
<td>Interface voltage: 3.3V</td>
<td>This interface is connected to the following devices: HDMI Transmitter AV17911, Video decoder AD17107, Audio codec: AK4952 (SO-8 BERMOS)</td>
</tr>
<tr>
<td></td>
<td>FC4</td>
<td>Interface voltage: 3.3V</td>
<td>This interface is connected to the following devices: Pin header (CN31): JW-HS002S-10-K</td>
</tr>
<tr>
<td></td>
<td>FC6</td>
<td>Interface voltage: 1.8V</td>
<td>EX0 Connector A (CN31: QSE-000-01F-D-A)</td>
</tr>
<tr>
<td></td>
<td>FC8</td>
<td>Interface voltage: 1.8V</td>
<td>This interface is connected to the following devices: PMIC DA9803, DA9810 (PM-3QC)</td>
</tr>
<tr>
<td>EX0 Connector</td>
<td>various modules</td>
<td>EX0 Connector A (CN31)</td>
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</tr>
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<td></td>
<td></td>
<td>EX0 Connector B (CN26) (For Ethernets B or VIN1)</td>
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</tr>
<tr>
<td></td>
<td></td>
<td>samtec 120pin QSG-00.01-F-D-A</td>
<td></td>
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<tr>
<td>Power IC</td>
<td></td>
<td>Internally Regulated: PO9308MPF (1V, 5V)</td>
<td>Dialog Semiconductor DA8910 (DV+) DVFS_1.0V, Core_1.0V)</td>
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<td></td>
<td></td>
<td>Dialog Semiconductor DA9063 (6V-&gt; 3.3V, 1.8V, 1.35V, Vcc SDH10, SDH12 power)</td>
<td>Dialog incorporated: ZLDO1101012DA (1.5V-&gt;1.2V)</td>
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<tr>
<td>Board size</td>
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<td>170mm x 125mm</td>
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1.2. Usage Notes

1.2.1. RZ/G1M Starter Kit Board Specifications

- **Take particular care to ensure the correct configurations of the jumpers and switches mounted on the RZ/G1M Starter Kit Board. Incorrect configurations may damage on-board devices.**

- **For the RZ/G1M Starter Kit Board, be sure to use the power supply that comes with it. Applying a voltage greater than 12 V may damage devices on the RZ/G1M Starter Kit Board.**

- **There are sequences for turning on and off the power supply to the RZ/G1M. For the RZ/G1M Starter Kit Board, be sure to obey the notes below.**

  1. **When power is turned on**
     - Be sure to confirm that the ACC switch (SW26) is off before plugging the AC adapter into the power source.
     - It is prohibited to plug the AC adapter into a power source while the ACC switch (SW26) is on.

  2. **When power is shut off**
     - Be sure to turn off the ACC switch (SW26) before unplugging the AC adapter from the power source.
     - It is prohibited to unplug the AC adapter from the power source while the ACC switch (SW26) is on.

- **The maximum current draw for the VSYS and D5.0V pins on the RZ/G1M Starter Kit Board is 7A each. Therefore, operation should be such that the current drawn by either pin does not exceed 7A. Also ensure that the current draw does not exceed 7A if an IO expansion board or external storage device is connected to the RZ/G1M Starter Kit Board.**
1.3. Board Configuration

The RZ/G1M Starter Kit Board is composed of a single board whose size is 170 mm × 125 mm. Figure 1.3.1 shows a block diagram of the RZ/G1M Starter Kit Board.

1.3.1. Block Diagram of RZ/G1M Starter Kit Board

Figure 1.3.1 Block Diagram of RZ/G1M Starter Kit Board
1.3.2. **Address Map of RZ/G1M Starter Kit Board**

For the DDR3L memory space, see the section DDR3L-SDRAM Interface.
For other address space, see the Hardware section in the RZ/G Series User's Manual.
2. RZ/G1M Starter Kit Board Interface Module Specifications

2.1. Mode Setting

2.1.1. Specifications

The operating mode of the RZ/G1M is set by a power-on reset. Each of the mode pins is set by pull up or pull down resistors, mounted on the development board. Several may also be changed by jumpers. For details on each operating mode, see the documents related to the RZ/G1M operating mode specifications.

2.1.1.1. MD0 Pin — Selection of Free-Running Mode or Step-Up Mode

This pin selects the free-running mode or step-up mode.

<table>
<thead>
<tr>
<th>MD0</th>
<th>Free-Running Mode or Step-Up Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Free-running mode (Fixed)</td>
</tr>
<tr>
<td>1</td>
<td>Step-up mode</td>
</tr>
</tbody>
</table>

2.1.1.2. MD[3:1] Pins — Selection of Boot Device

These pins select the boot device.

<table>
<thead>
<tr>
<th>MD3</th>
<th>MD2</th>
<th>MD1</th>
<th>Selection of Boot Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Boot from area 0 (boot from the external mask ROM)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>QSPI (48.75 MHz/16-Kbyte transfer) (Fixed)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Reserved</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>Reserved</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>QSPI (39 MHz/16-Kbyte transfer)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>Reserved</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>QSPI (39 MHz/4-Kbyte transfer)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

2.1.1.3. MD4 Pin — Selection of CS0 Space Size

This pin selects whether the area 0 space (CS0) is used as a normal space (64 Mbytes) or an expanded space (128 Mbytes).

<table>
<thead>
<tr>
<th>MD4</th>
<th>Area Division</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Area 0: 64 Mbytes (Fixed... Area0 not used)</td>
</tr>
<tr>
<td>1</td>
<td>Area 0: 128 Mbytes</td>
</tr>
</tbody>
</table>

2.1.1.4. MD5 Pin — Selection of Secure or Non-Secure Mode

This pin selects the secure or non-secure mode.

<table>
<thead>
<tr>
<th>MD5</th>
<th>Selection of Secure or Non-Secure Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Secure (When LCS = Secure, the value read from the register for MD5 is forcibly set to 0.)</td>
</tr>
<tr>
<td>1</td>
<td>Non-secure (Default)</td>
</tr>
</tbody>
</table>

2.1.1.5. MD[7:6] Pins — Selection of Master Boot Processor

These pins select the master boot processor.

<table>
<thead>
<tr>
<th>MD7</th>
<th>MD6</th>
<th>Selection of Master Boot Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>CA15 boot (Fixed)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Reserved</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>SH boot (32 bits)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

2.1.1.6. MD8 Pin — Selection of Area 0 Space Data Bus Width

This pin sets the data bus width of the area 0 space (CS0) to 8 bits or 16 bits. Select the data bus width of the boot device connected to the LBSC.

<table>
<thead>
<tr>
<th>MD8</th>
<th>EXBUS Area 0 Data Bus Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>8-bit bus (Fixed... Area0 not used)</td>
</tr>
<tr>
<td>1</td>
<td>16-bit bus</td>
</tr>
</tbody>
</table>
2.1.1.7. MD9 Pin — Selection of Crystal Resonator or Crystal Oscillator

This pin selects either a crystal resonator or a crystal oscillator to be connected to the EXTAL/XTAL pins. A crystal oscillator (X6: 20 MHz) is mounted on the RZ/G1M Starter Kit Board by default. The crystal resonator (X5) and its peripheral circuit are not mounted.

<table>
<thead>
<tr>
<th>MD9</th>
<th>EXTAL/XTAL Pin Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>An external clock is input to the EXTAL pin. (Fixed)</td>
</tr>
<tr>
<td>1</td>
<td>A crystal resonator is connected to the EXTAL and XTAL pins.</td>
</tr>
</tbody>
</table>

2.1.1.8. MD12 — Reserved

Do not change the initial setting at shipment (MD12 = 0).

2.1.1.9. MD21, MD20, MD11, MD10, and MDT[1:0] Pins — Switching of JTAG, SDHI1, and SDHI2

These pins select the debugging function through the JTAG connector (CN1) or the SD card slot. Debugging through SDHI1 or SDHI2 is possible by the combination of MD pin settings in the RZ/G1M specifications, but not available on the RZ/G1M Starter Kit Board.

<table>
<thead>
<tr>
<th>MD10</th>
<th>MD[21:20]</th>
<th>MD11</th>
<th>MDT[1:0]</th>
<th>JTAG</th>
<th>SDHI1</th>
<th>SDHI2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>00</td>
<td>-</td>
<td>--</td>
<td>Coresight (*1)</td>
<td>Normal function</td>
<td>Normal function</td>
</tr>
<tr>
<td>0</td>
<td>00</td>
<td>0</td>
<td>00</td>
<td>Coresight (*1)</td>
<td>Tensilica</td>
<td>Normal function</td>
</tr>
<tr>
<td>0</td>
<td>00</td>
<td>1</td>
<td>01</td>
<td>Coresight (*1)</td>
<td>SH-X4</td>
<td>Normal function</td>
</tr>
<tr>
<td>0</td>
<td>00</td>
<td>1</td>
<td>10</td>
<td>Coresight (*1)</td>
<td>Normal function</td>
<td>Tensilica</td>
</tr>
<tr>
<td>0</td>
<td>00</td>
<td>1</td>
<td>11</td>
<td>Coresight (*1)</td>
<td>Normal function</td>
<td>SH-X4</td>
</tr>
<tr>
<td>0</td>
<td>11</td>
<td>0</td>
<td>--</td>
<td>SH-X4</td>
<td>Normal function</td>
<td>Normal function</td>
</tr>
<tr>
<td>0</td>
<td>11</td>
<td>0</td>
<td>00</td>
<td>SH-X4</td>
<td>Coresight (*1)</td>
<td>Normal function</td>
</tr>
<tr>
<td>1</td>
<td>01</td>
<td>0</td>
<td>--</td>
<td>Coresight (*1)</td>
<td>Normal function</td>
<td>Normal function</td>
</tr>
<tr>
<td>1</td>
<td>01</td>
<td>1</td>
<td>00</td>
<td>Coresight (*1)</td>
<td>GPS</td>
<td>Normal function</td>
</tr>
<tr>
<td>1</td>
<td>01</td>
<td>1</td>
<td>01</td>
<td>Coresight (*1)</td>
<td>SH-X4</td>
<td>Normal function</td>
</tr>
<tr>
<td>1</td>
<td>10</td>
<td>0</td>
<td>--</td>
<td>SH-X4</td>
<td>Normal function</td>
<td>Normal function</td>
</tr>
</tbody>
</table>

(*1) “Coresight” is an abbreviation of “Coresight debug port”.

2.1.1.10. MD[14:13] Pins — Frequency Mode Setting

These pins select the frequency mode. A crystal oscillator (X6: 20 MHz) is mounted on the RZ/G1M Starter Kit Board.

Do not change the initial setting at shipment (MD14 = 0, MD13 = 1).

<table>
<thead>
<tr>
<th>MD14</th>
<th>MD13</th>
<th>EXTAL Frequency</th>
<th>EXTAL Divider</th>
<th>PLL1 (CPGM Main)</th>
<th>PLL0 (CPGM)</th>
<th>PLL3 DDR1600/DDR1333</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>15 MHz</td>
<td>× 1/1</td>
<td>×208 VCO = 3120 MHz</td>
<td>×172 VCO = 1290 MHz</td>
<td>×106/×88 VCO = 1590 MHz/1320 MHz</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>20 MHz</td>
<td>× 1/1</td>
<td>×156 VCO = 3120 MHz</td>
<td>×130 VCO = 1300 MHz</td>
<td>×80/×66 VCO = 1600 MHz/1320 MHz</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>25 MHz</td>
<td>× 1/2</td>
<td>×240 VCO = 3120 MHz</td>
<td>×200 VCO = 1300 MHz</td>
<td>×122/×102 VCO = 1586 MHz/1326 MHz</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>30 MHz</td>
<td>× 1/2</td>
<td>×208 VCO = 3120 MHz</td>
<td>×172 VCO = 1290 MHz</td>
<td>×106/×88 VCO = 1590 MHz/1320 MHz</td>
</tr>
</tbody>
</table>

2.1.1.11. MD19 Pin — Selection of DDR3-SDRAM Bus Clock

This pin selects the frequency of the DDR3-SDRAM bus clock.

<table>
<thead>
<tr>
<th>MD19</th>
<th>Switching of DDR Clock</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>DDR3-1600 mode</td>
</tr>
<tr>
<td>1</td>
<td>DDR3-1333 mode</td>
</tr>
</tbody>
</table>
2.1.1.12. MD28, MD27, and MD22 Pins — Selection of DDR Mode and MTSB Mode

These pins select the DDR3-SDRAM interface mode and MTSB mode.

<table>
<thead>
<tr>
<th>MD28</th>
<th>MD27</th>
<th>MD22</th>
<th>DDR 64 Bits/32 Bits</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>DDR 64 bits x 1ch</td>
<td>-</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>DDR 64 bits x 1ch</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>DDR 32 bits x 1ch</td>
<td>User PinMAX</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>DDR 64 bits x 1ch</td>
<td>User PinMAX</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>DDR 32 bits x 1ch</td>
<td>User PinMAX</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>DDR 32 bits x 2ch</td>
<td>(Fixed)</td>
</tr>
</tbody>
</table>

Note: The MD28, MD27, and MD22 pins are fixed to "1" on the board.

2.1.1.13. MD23 Pin — Selection of SATA0 or USB3.0 Function

This pin selects the SATA0 or USB3.0 function. MD23 is fixed to "0" on the RZ/G1M Starter Kit Board.

<table>
<thead>
<tr>
<th>MD23</th>
<th>Selection of SATA0 or USB3.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>SATA0 (Fixed)</td>
</tr>
<tr>
<td>1</td>
<td>USB3.0</td>
</tr>
</tbody>
</table>

2.1.1.14. MD24 Pin — Selection of SATA1 or PCIE Function

This pin selects the SATA1 or PCIE function. MD24 is fixed to "1" on the RZ/G1M Starter Kit Board.

<table>
<thead>
<tr>
<th>MD24</th>
<th>Selection of SATA1 or PCIE</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>SATA1</td>
</tr>
<tr>
<td>1</td>
<td>PCIE (Fixed)</td>
</tr>
</tbody>
</table>

2.1.2. Initial Values of Mode Setting Pins on RZ/G1M Starter Kit Board

<table>
<thead>
<tr>
<th>MD Pins</th>
<th>Initial Value</th>
<th>Initial Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>MD0</td>
<td>0</td>
<td>Free-running mode</td>
</tr>
<tr>
<td>MD[3:1]</td>
<td>010</td>
<td>Boot from QSPI</td>
</tr>
<tr>
<td>MD4</td>
<td>0</td>
<td>CS0 space size (64 Mbytes)</td>
</tr>
<tr>
<td>MD5</td>
<td>1</td>
<td>Non-secure mode</td>
</tr>
<tr>
<td>MD[7:6]</td>
<td>00</td>
<td>Cortex-A15 boot</td>
</tr>
<tr>
<td>MD8</td>
<td>0</td>
<td>CS0 space data bus width (16 bits)</td>
</tr>
<tr>
<td>MD9</td>
<td>0</td>
<td>Crystal oscillator is used.</td>
</tr>
<tr>
<td>MD12</td>
<td>0</td>
<td>-</td>
</tr>
<tr>
<td>MD10, MD[21:20], MD11, MDT[1:0]</td>
<td>0,10,0,00</td>
<td>JTAG (CN1) = Boundary SCAN SDHI1 and SDHI2 = Normal function</td>
</tr>
<tr>
<td>MD[14:13]</td>
<td>01</td>
<td>Input frequency = 20 MHz</td>
</tr>
<tr>
<td>MD19</td>
<td>0</td>
<td>DDR3-1600 mode</td>
</tr>
<tr>
<td>MD28, MD27, MD22</td>
<td>111</td>
<td>DDR 32 bits x 2ch</td>
</tr>
<tr>
<td>MD23</td>
<td>0</td>
<td>SATA0</td>
</tr>
<tr>
<td>MD24</td>
<td>1</td>
<td>PCIE</td>
</tr>
</tbody>
</table>
2.1.3. Multiplexing and Method of Setting for Mode Setting Pins

The following table covers the pin functions that are multiplexed with the mode pins of the RZ/G1M, and how the individual mode pins are set. For the mode pins that are used with fixed values, resistors are used to set them to their fixed values according to the initial settings in table 2.1.1, Initial Values of RZ/G1M Mode Setting Pins on RZ/G1M Starter Kit Board. Such mode pins are described as “Fixed by a resistor” in the Setting Method column in the table below.

<table>
<thead>
<tr>
<th>MD Pin</th>
<th>Pin Function</th>
<th>Strapping Options</th>
<th>Setting Method</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>MD0</td>
<td>DU1_CDE (GPIO)</td>
<td>Free-running (0)/Step-up (1)</td>
<td>Fixed by resistor</td>
<td>Pulled-down (0)</td>
</tr>
<tr>
<td>MD1</td>
<td>DU1_DISP</td>
<td>Selects boot device</td>
<td>Fixed by resistor</td>
<td>Pulled-down (0)</td>
</tr>
<tr>
<td>MD2</td>
<td>DU1_VSYNC</td>
<td>Fixed by resistor</td>
<td>Pulled-up (1)</td>
<td></td>
</tr>
<tr>
<td>MD3</td>
<td>DU1_HSYNC</td>
<td>Fixed by resistor</td>
<td>Pulled-down (0)</td>
<td></td>
</tr>
<tr>
<td>MD4</td>
<td>WE1#</td>
<td>Selects area 0 size</td>
<td>Fixed by resistor</td>
<td>Pulled-down (0)</td>
</tr>
<tr>
<td>MD5</td>
<td>AUDIO_CLKOUT (GPIO)</td>
<td>Secure (0) or non-secure (1)</td>
<td>Fixed by resistor</td>
<td>PULLED-UP(1)</td>
</tr>
<tr>
<td>MD6</td>
<td>WE0#</td>
<td>Selects boot processor</td>
<td>Fixed by resistor</td>
<td>Pulled-down (0)</td>
</tr>
<tr>
<td>MD7</td>
<td>DACK0 (GPIO)</td>
<td>Fixed by resistor</td>
<td>Pulled-down (0)</td>
<td></td>
</tr>
<tr>
<td>MD8</td>
<td>EX_CS5# (GPIO)</td>
<td>Fixed by a resistor</td>
<td>Pulled-down (0)</td>
<td></td>
</tr>
<tr>
<td>MD9</td>
<td>EX_CS3# (GPIO)</td>
<td>Fixed by a resistor</td>
<td>Pulled-down (0)</td>
<td></td>
</tr>
<tr>
<td>MD10</td>
<td>BS#</td>
<td>Debugging mode</td>
<td>Fixed by resistor</td>
<td>Pulled-down (0)</td>
</tr>
<tr>
<td>MD11</td>
<td>DU1_DB5</td>
<td>Fixed by resistor</td>
<td>Pulled-down (0)</td>
<td></td>
</tr>
<tr>
<td>MD12</td>
<td>RD#</td>
<td>Fixed by resistor</td>
<td>Pulled-down (0)</td>
<td></td>
</tr>
<tr>
<td>MD13</td>
<td>A3</td>
<td>Selects frequency mode</td>
<td>Fixed by a resistor</td>
<td>Pulled-up (1)</td>
</tr>
<tr>
<td>MD14</td>
<td>A19</td>
<td>Fixed by a resistor</td>
<td>Pulled-down (0)</td>
<td></td>
</tr>
<tr>
<td>MD15</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>MD16</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>MD17</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>MD18</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>MD19</td>
<td>A14</td>
<td>DDR clock 1600/1333</td>
<td>Fixed by resistor</td>
<td>Pulled-down (0)</td>
</tr>
<tr>
<td>MD20</td>
<td>A15</td>
<td>Debugging mode</td>
<td>Fixed by resistor</td>
<td>Pulled-down (0)</td>
</tr>
<tr>
<td>MD21</td>
<td>A13</td>
<td>Fixed by resistor (JP9 off)</td>
<td>PULLED-UP(1)</td>
<td></td>
</tr>
<tr>
<td>MD22</td>
<td>A10</td>
<td>DDR, MTSB mode</td>
<td>Fixed by a resistor</td>
<td>Pulled-up (1)</td>
</tr>
<tr>
<td>MD23</td>
<td>A2</td>
<td>Selects SATA0/USB3.0</td>
<td>Fixed by a resistor</td>
<td>Pulled-down (0)</td>
</tr>
<tr>
<td>MD24</td>
<td>A4</td>
<td>Selects SATA1/PCIE</td>
<td>Fixed by a resistor</td>
<td>Pulled-up (1)</td>
</tr>
<tr>
<td>MD25</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>MD26</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>MD27</td>
<td>A7</td>
<td>DDR, MTSB mode</td>
<td>Fixed by a resistor</td>
<td>Pulled-up (1)</td>
</tr>
<tr>
<td>MD28</td>
<td>A1</td>
<td>Fixed by a resistor</td>
<td>Pulled-up (1)</td>
<td></td>
</tr>
<tr>
<td>MDT0</td>
<td>SIM0_CLK</td>
<td>Debugging mode</td>
<td>Fixed by resistor</td>
<td>Pulled-down (0)</td>
</tr>
<tr>
<td>MDT1</td>
<td>SIM0_RST</td>
<td>Fixed by resistor</td>
<td>Pulled-down (0)</td>
<td></td>
</tr>
</tbody>
</table>
2.1.4. Block Diagram of Peripheral Circuit for Mode Pins

On the RZ/G1M Starter Kit Board, pull-up (100 kΩ) and pull-down (10 kΩ) resistors are used to implement the settings of the mode pins that are largely used with fixed values. When changes to the settings of mode pins are likely, this can be implemented by switches which, through resistive voltage division, select the low level when turned on and the high level when turned off.

When the RZ/G1M is released from the power-on reset (when the PRESET# signal of the RZ/G1M is changed from low to high), the mode value set by the switch or resistive voltage division is input to the RZ/G1M.

![Block Diagram of Peripheral Circuit for Mode Pins on RZ/G1M Starter Kit Board](image)

**Figure 2.1.1 Peripheral Circuit for Mode Pins on RZ/G1M Starter Kit Board**
2.2. DDR3L-SDRAM Interface

2.2.1. Specifications

The RZ/G1M Starter Kit Board incorporates four 4-Gbit DDR3-SDRAMs (16-bit bus width) (DDR: 32 bits × 2 channels) and operates at a maximum speed of DDR3-1600. On the RZ/G1M Starter Kit Board, the RZ/G1M and DDR3-SDRAMs are connected in 32-bit × 2-channel mode; the DDR3-SDRAMs on the channel 0 side are allocated to the address space from H'01_0000 0000 to H'01_3FFF FFFF and those on the channel 1 side are allocated to the address space from H'02_0000 0000 to H'02_3FFF FFFF. The address ranges from H'00_4000 0000 to H'00_7FFF FFFF can be accessed by default as a mirror area of H'01_0000 0000 to H'01_3FFF FFFF.

<table>
<thead>
<tr>
<th>Table 2.2.1 DDR3L-SDRAM Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interface</td>
</tr>
<tr>
<td>Product name</td>
</tr>
<tr>
<td>Power supply voltage</td>
</tr>
<tr>
<td>Capacity</td>
</tr>
<tr>
<td>Channel 0:</td>
</tr>
<tr>
<td>Channel 1:</td>
</tr>
<tr>
<td>Bus width</td>
</tr>
<tr>
<td>Memory bus frequency (RZ/G1M spec.)</td>
</tr>
</tbody>
</table>

Note:
To access the address spaces for channels 0 and 1 as a single consecutive area, register settings are necessary. For details, refer to the RZ/G1M documentation.
### 2.2.2. Signal Correlation

#### Table 2.2.2 DDR3L-SDRAM Signal Correlation

<table>
<thead>
<tr>
<th>RZ/G1M (DDR 32 bits × 2ch)</th>
<th>DDR3L-SDRAM</th>
<th>Channel 1</th>
<th>Channel 0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Channel 1</td>
<td>Channel 0</td>
<td></td>
</tr>
<tr>
<td>M1DQ[15:0]</td>
<td>DQ[7:0]</td>
<td>DQ[7:0]</td>
<td>-</td>
</tr>
<tr>
<td>M0DQ[31:16]</td>
<td>-</td>
<td></td>
<td>D[15:0]</td>
</tr>
<tr>
<td>M0DQ[15:0]</td>
<td>-</td>
<td></td>
<td>DQ[7:0]</td>
</tr>
<tr>
<td>M0BA[2:0]</td>
<td>-</td>
<td></td>
<td>BA[2:0]</td>
</tr>
<tr>
<td>M1CK1, M1CK1#</td>
<td>CK, CK#</td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>M1CK0, M1CK0#</td>
<td>-</td>
<td>CK, CK#</td>
<td></td>
</tr>
<tr>
<td>M0CK1, M0CK1#</td>
<td>-</td>
<td>CK, CK#</td>
<td></td>
</tr>
<tr>
<td>M0CK0, M0CK0#</td>
<td>-</td>
<td>-</td>
<td>CK, CK#</td>
</tr>
<tr>
<td>M1CE1</td>
<td>CKE</td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>M1CE0</td>
<td>-</td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>M0CE0</td>
<td>-</td>
<td></td>
<td>CKE</td>
</tr>
<tr>
<td>M1CS1#</td>
<td>CS#</td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>M1CS0#</td>
<td>-</td>
<td>CS#</td>
<td></td>
</tr>
<tr>
<td>M0CS1#</td>
<td>-</td>
<td>-</td>
<td>CS#</td>
</tr>
<tr>
<td>M0CS0#</td>
<td>-</td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>M1WE#</td>
<td>WE#</td>
<td></td>
<td>WE#</td>
</tr>
<tr>
<td>M0WE#</td>
<td>-</td>
<td></td>
<td>WE#</td>
</tr>
<tr>
<td>M1RAS#</td>
<td>RAS#</td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>M0RAS#</td>
<td>RAS#</td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>M1CAS#</td>
<td>CAS#</td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>M0CAS#</td>
<td>-</td>
<td>CAS#</td>
<td></td>
</tr>
<tr>
<td>M1DS[3:2], M1DS[3:2]#</td>
<td>DQSU, DQSL</td>
<td>-</td>
<td>DQSU, DQSL</td>
</tr>
<tr>
<td>M1DS[1:0], M1DS[1:0]#</td>
<td>-</td>
<td>DQSU, DQSL</td>
<td>DQSU, DQSL</td>
</tr>
<tr>
<td>M0DS[3:2], M0DS[3:2]#</td>
<td>-</td>
<td>-</td>
<td>DQSU, DQSL</td>
</tr>
<tr>
<td>M0DS[1:0], M0DS[1:0]#</td>
<td>-</td>
<td>-</td>
<td>DQSU, DQSL</td>
</tr>
<tr>
<td>M1DM[3:2]</td>
<td>DMU, DML</td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>M1DM[1:0]</td>
<td>-</td>
<td>DMU, DML</td>
<td></td>
</tr>
<tr>
<td>M0DM[3:2]</td>
<td>-</td>
<td>DMU, DML</td>
<td></td>
</tr>
<tr>
<td>M0DM[1:0]</td>
<td>-</td>
<td>-</td>
<td>DMU, DML</td>
</tr>
<tr>
<td>M1ODT#</td>
<td>ODT</td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>M0ODT#</td>
<td>-</td>
<td>ODT</td>
<td></td>
</tr>
<tr>
<td>M1RESET#</td>
<td>RESET#</td>
<td></td>
<td>RESET#</td>
</tr>
<tr>
<td>M0RESET#</td>
<td>-</td>
<td>RESET#</td>
<td>RESET#</td>
</tr>
</tbody>
</table>

(*) DDR\_VDD/2 [V] is supplied to the M0VREFDQ[1:0] and M1VREFDQ[1:0] pins of the RZ/G1M.
2.2.3. Block Diagram

The following figure shows a block diagram of the DDR3-SDRAM interface.

![Block Diagram of DDR3-SDRAM Interface](image-url)
2.3. SPI-FLASH Interface (QSPI)

2.3.1. Specifications

The RZ/G1M Starter Kit board incorporates 512-Mbit and 32-Mbit SPI flash memory devices manufactured by Spansion. These SPI flash memory devices are connected to the QSPI of the RZ/G1E via jumper JP2. When the 512-Mbit SPI flash memory (U16) is to be accessed, set JP2 to pin 1 side, and when the 32-Mbit SPI flash memory (U579) is to be accessed, set JP2 to the pin 3 side.

Since the loader and mini-monitor are stored in the lower-order address space of the SPI flash memory (U579, 32 Mbits), do not modify the contents of this area. The contents of the SPI flash memory (U16, 512 Mbits) can be modified as required.

![Table 2.3.1 Flash Memory Specifications](image)

<table>
<thead>
<tr>
<th>QSPI controller</th>
<th>RZ/G1M's on-chip QSPI module</th>
</tr>
</thead>
</table>
| SPI flash memory | (1) U16: Spansion S25FL512SAGMFIG11 (512 Mbits)  
(2) U579: Spansion S25FL032P0XMFI011 (32 Mbits) |
| Clock rate of RZ/G1M's QSPI | 48.75-MHz operation (max.) |

2.3.2. Block Diagram

A block diagram of the SPI flash memory interface is shown below.

![Figure 2.3.1 Block Diagram of SPI-Flash Interface](image)
2.4. Video Input Interface

2.4.1. Specifications

On the RZ/G1M Starter Kit Board, ADV7180WBCP32Z (U22) manufactured by Analog Devices is connected to VIN0 of the RZ/G1M and used as a composite video decoder. The ADV7180WBCP32Z (U22) handles inputs in the ITU-R BT.656 8-bit (YCbCr) format according to the switch settings. The block diagram of the VIN0 interface is shown below.

The registers of ADV7180 should be set via channel 2 of the I2C.

<table>
<thead>
<tr>
<th>Video input module</th>
<th>RZ/G1M’s on-chip video input module channel 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Composite video decoder for VIN1</td>
<td>U22: ADV7180WBCP32Z by Analog Devices</td>
</tr>
<tr>
<td>I²C-BUS ch2 slave address</td>
<td>H’40 for write, H’41 for read</td>
</tr>
</tbody>
</table>

| Video input connector | CN: RCA connector for VIN1 |

2.4.2. Block Diagram

![Figure 2.4.1 Block Diagram of Video Input Interface](image)

**Table 2.4.1 Video Input Specifications**
2.5. Video Output Interface

2.5.1. Specifications

The RZ/G1M Starter Kit Board incorporates one display unit (DU) with the LVDS interface and one display unit with the digital RGB interface.

On the RZ/G1M Starter Kit Board, the HDMI transmitter (ADV7511) converts the digital RGB signals of DU1 to HDMI signals. These digital RGB signals are also connected to the EXIO connector (CN30). In addition, the LCD connector (CN30) is directly connected to DU_LVDS channel 0 (DU0_LVDS).

<table>
<thead>
<tr>
<th>Display controller</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>DU0_LVDS</td>
<td>LVDS Output</td>
</tr>
<tr>
<td></td>
<td>Connector CN30: DF14A-20P-1.25H by Hirose, for LVDS signals.</td>
</tr>
<tr>
<td></td>
<td>CN31: Backlight control and I2C / interrupt input for touch.</td>
</tr>
<tr>
<td>DU1 (digital RGB)</td>
<td>HDMI Output</td>
</tr>
<tr>
<td></td>
<td>HDMI transmitter converts digital RGB signals to HDMI signals.</td>
</tr>
<tr>
<td></td>
<td>U44: ADV7511WBSWZ by Analog Devices</td>
</tr>
<tr>
<td></td>
<td>Connector CN45: HMNF-195N-4BH90 (HDMI type A, standard, 19-pin) by Accurate Innotech</td>
</tr>
</tbody>
</table>
2.5.2. Block Diagram

A block diagram of the video output interface on the RZ/G1M Starter Kit Board is shown below.

![Block Diagram of Video Output Interface](image)

**Figure 2.5.1 Block Diagram of Video Output Interface**
2.6. Debugger Interface

2.6.1. Specifications

The RZ/G1M Starter Kit Board incorporates a debugger interface via a 20-pin connector (DBG) for connection to the JTAG emulator. The RZ/G1M supports the DBG3 interface as a debugger interface, but the RZ/G1M Starter Kit Board does not include this function. The signals related to DBG3 (SDHI2) are instead connected to EXIO connector. On the RZ/G1M Starter Kit Board, the debugging function can be accessed through the JTAG connector CN1. **(Attention) If use as ARM Coresight debug port, remove JP9 jumper off.**

<table>
<thead>
<tr>
<th>DBG interface (20-pin)</th>
<th>CN1: HTST-110-01-S-DV by Samtec</th>
</tr>
</thead>
</table>

2.6.2. Block Diagram

![Diagram of JTAG (DBG) Interface](image)

**Figure 2.6.1 Block Diagram of JTAG (DBG) Interface**
2.7. Debug Ether Interface (EtherMAC)

2.7.1. Specifications

The RZ/G1M Starter Kit Board incorporates the EtherMAC that supports 100Base-T or 10Base-T compliant with IEEE 802.3u. On the RZ/G1M Starter Kit Board, the EtherMAC signals are connected to the RMII PHY interface (KSZ8041RNLI) manufactured by Micrel. In addition, CN3 on the bottom of the board supports the REACH interface sub boards.

Table 2.7.1 Debug Ether Interface Specifications

<table>
<thead>
<tr>
<th></th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAC layer</td>
<td>RZ/G1M's on-chip EtherMAC</td>
</tr>
<tr>
<td>Physical layer transceiver</td>
<td>U21: KSZ8041RNLI (RMII) by Micrel</td>
</tr>
<tr>
<td>Reach connector</td>
<td>CN3  (as EtherAVB)</td>
</tr>
<tr>
<td>Modular connector</td>
<td>CN10: CWKRJ-13BNL (RJ-45 with pulse transformer) by CWE</td>
</tr>
</tbody>
</table>

2.7.2. Block Diagrams

A block diagram of the debug Ether interface is shown below.

![Block Diagram of Debug Ether Interface](image-url)
2.8. Audio Codec Interface (SSI0, SSI1, SSI2, and SSI9)

2.8.1. Specifications

On the RZ/G1M Starter Kit Board, the codec (AK4642EN) is connected to the SSI0 and SSI1 of the RZ/G1M. The PDN (power-down) pin of AK4643EN is controlled by the PRESETOUT# signal output from the RZ/G1M.

The audio interface of AK4642EN is in the slave mode after PRESETOUT# is released from a reset and can be switched to the master mode by a register that is accessed via channel 2 of the I2C. Furthermore, the SSI on the RZ/G1M side can be set as the master or a slave. It is assumed that SSI_SDATA0 is set to transmit mode and SSI_SDATA1 is set to receive mode on the RZ/G1M Starter Kit Board.

Among the signals of the audio interface, the signals of SSI0, SSI1, SSI2, and SSI9 are also connected to HDMI transmitter ADV7511 (U44) on the RZ/G1M Starter Kit Board.

<table>
<thead>
<tr>
<th>Controller</th>
<th>RZ/G1M’s on-chip SSI0 and SSI1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Codec</td>
<td>U24: AK4642EN by Asahi Kasei</td>
</tr>
<tr>
<td>Audio interface</td>
<td>RZ/G1M (SSI) = Master or slave selectable</td>
</tr>
<tr>
<td></td>
<td>AK4642EN = Master or slave selectable (default: slave)</td>
</tr>
<tr>
<td>Audio connector</td>
<td>LINE-OUT CN13, 3.5-mm green mini-jack</td>
</tr>
<tr>
<td></td>
<td>LINE-IN/MIC-IN CN14 3.5-mm pink mini-jack</td>
</tr>
</tbody>
</table>

Table 2.8.1 SSI Codec Specifications

2.8.2. Block Diagram

![Figure 2.8.1 Block Diagram of Audio Codec Interface](image_url)
2.9. PCI-Express Interface

2.9.1. Specifications

The RZ/G1M Starter Kit Board incorporates the PCI-Express interface for one lane (×1) as a dedicated interface for the PCI-Express bus. The on-chip PCIE module in the RZ/G1M works in either of two modes, Root Port or Endpoint, which are defined in the PCI Express specifications. In the RZ/G1M, the operating mode is specified through internal register settings (mode setting register (PCIEMSR)). For details, refer to the RZ/G Series User’s Manual: Hardware.

Note:
To reduce the difference in wiring length between each pair of differential signals from the RZ/G1M to the PCI-Express slot, the D+ and D- line automatic swap function is used to swap the TODP1_PCIE and TODN1_PCIE signals output from the transmit pins before connection to the slot.

Table 2.9.1 PCI-Express Interface Specifications

<table>
<thead>
<tr>
<th>Description</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCI-Express controller</td>
<td>RZ/G1M’s on-chip PCI-Express controller</td>
</tr>
<tr>
<td>PCI-Express slot (1 lane)</td>
<td>JPCIE-4CEEB36XRT110 by Weknowtechnology (CN5)</td>
</tr>
<tr>
<td>PCI-Express clock source</td>
<td>IDT5V41066PGGI by IDT</td>
</tr>
</tbody>
</table>

2.9.2. Block Diagram

![Block Diagram of PCI-Express Interface](image)

Figure 2.9.1 Block Diagram of PCI-Express Interface
2.10. Serial-ATA Interface

2.10.1. Specifications

The RZ/G1M Starter Kit Board incorporates one serial-ATA interface (SATA0) channel. The RZ/G1M's on-chip serial-ATA interface conforms to the Serial ATA standard rev. 3.1 and supports transfer rates of 1.5 Gbps (Gen1) and 3.0 Gbps (Gen2). The RZ/G1M Starter Kit Board incorporates a 4-pin power connector (CN2) for the ATAPI device. The power connector conversion cable (4-pin to 15-pin) is required to supply power to the SATA device.

<table>
<thead>
<tr>
<th>Table 2.10.1 Serial-ATA Interface Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Serial-ATA interface controller</td>
</tr>
<tr>
<td>Serial-ATA connector (signal)</td>
</tr>
<tr>
<td>Serial-ATA clock source</td>
</tr>
</tbody>
</table>

2.10.2. Block Diagram

![Figure 2.10.1 Block Diagram of Serial-ATA Interface](image)

2.10.3. PCI-Express and Serial-ATA Clock Source Unit

The details on the clock source unit of the PCI-Express interface and serial-ATA interface are shown below. IDT5V41066PGGI manufactured by IDT is used for the clock driver. This clock driver multiplies the input frequency (25 MHz) to supply a 100-MHz differential clock to the RZ/G1M and PCI-Express slot.

Note:
To reduce the difference in wiring length between each pair of differential signals from the RZ/G1M to the clock source, the P and N lines from the clock pins (CICREFP0_SATA/PCIe_18 and CICREFN0_SATA/PCIe_18 signals) are swapped before connection to the clock source.

![Figure 2.10.2 Block Diagram of PCI-Express and Serial-ATA Clock Source](image)
2.11. SD Card Host Interface 0 (SDHI0)

2.11.1. Specifications

The RZ/G1M Starter Kit Board incorporates an SD card slot (CN8) for the on-chip SD card host interface (SDHI0) of the RZ/G1M. For details on the SDHI0, see the RZ/G Series User’s Manual: Hardware.

On the RZ/G1M Starter Kit Board, the interface voltage (VCCQ_SD0) of the SD card slot can be selected by GP2_12. When GP2_12 is set to 1, 3.3 V is supplied as VCCQ_SD0. When GP2_12 is set to 0, 1.8 V is supplied as VCCQ_SD0.

<table>
<thead>
<tr>
<th>SD card host interface</th>
<th>RZ/G1M’s on-chip SD card host interface channel 0 (SDHI0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interface voltage control</td>
<td>VCCQ_SD0 = 3.3 V (GP2_12 = ‘1’)</td>
</tr>
<tr>
<td></td>
<td>VCCQ_SD0 = 1.8 V (GP2_12 = ‘0’)</td>
</tr>
<tr>
<td>SD card slot</td>
<td>SDC009-A0-0003 by PROCONN (CN8)</td>
</tr>
</tbody>
</table>

2.11.2. Block Diagram

![Block Diagram of SD Card Host Interface (SDHI0)](image-url)

*Figure 2.11.1 Block Diagram of SD Card Host Interface (SDHI0)*
2.12. SD Card Host Interface 2 (SDHI2)

2.12.1. Specifications

The RZ/G1M Starter Kit Board incorporates a microSD card slot (CN9) for the on-chip SD card host interface (SDHI2) of the RZ/G1M. For details on the SDHI2, see the RZ/G Series User’s Manual: Hardware.

On the RZ/G1M Starter Kit Board, the interface voltage (VCCQ_SD2) of the microSD card slot can be selected by GP2_26. When GP2_26 is set to 1, 3.3 V is supplied as VCCQ_SD2. When GP2_26 is set to 0, 1.8 V is supplied as VCCQ_SD2.

<table>
<thead>
<tr>
<th>SD card host interface</th>
<th>RZ/G1M’s on-chip SD card host interface channel 2 (SDHI2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interface voltage control</td>
<td>VCCQ_SD2 = 3.3 V (GP2_26 = ‘1’)</td>
</tr>
<tr>
<td></td>
<td>VCCQ_SD2 = 1.8 V (GP2_26 = ‘0’)</td>
</tr>
<tr>
<td>microSD card slot</td>
<td>MSPN09-A0-1002 by PROCONN (CN9)</td>
</tr>
</tbody>
</table>

2.12.2. Block Diagram

![Block Diagram of SD Card Host Interface (SDHI2)](image)

Figure 2.12.1 Block Diagram of SD Card Host Interface (SDHI2)
2.13. USB2.0 Interface

2.13.1. Specifications

The RZ/G1M Starter Kit Board has two USB2.0 ports that can be used as two USB2.0 host interface ports or one USB2.0 host interface port and one USB2.0 function interface port. The function interface is supported in channel 0. The RZ/G1M Starter Kit Board incorporates a micro-AB connector as CN22 and a type A connector as CN7. For details, see the USB specifications in the RZ/G Series User’s Manual:Hardware and related datasheets.

Table 2.13.1 USB2.0 Specifications

<table>
<thead>
<tr>
<th>Description</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB controller</td>
<td>RZ/G1M’s on-chip USB2.0 host and function controller</td>
</tr>
<tr>
<td>USB power supply</td>
<td>BD6516F by ROHM</td>
</tr>
<tr>
<td></td>
<td>Current limit: 2.4 [A]</td>
</tr>
<tr>
<td>USB host CN</td>
<td>RZ/G1M USB CH1 CN7: Type A connector</td>
</tr>
<tr>
<td></td>
<td>67643-3911 by Molex</td>
</tr>
<tr>
<td>USB host/function CN</td>
<td>RZ/G1M USB CH0 CN22: micro-AB connector</td>
</tr>
<tr>
<td></td>
<td>KS-MCR-AB01N3- by Weknowtechnology</td>
</tr>
<tr>
<td>ESD protection diode</td>
<td>HZD6.2Z4 by Renesas</td>
</tr>
<tr>
<td>Common mode filter</td>
<td>DLP11SN900HL2 by Murata</td>
</tr>
<tr>
<td>Chip beads</td>
<td>BLM18PG330SN1D by Murata</td>
</tr>
</tbody>
</table>

* The connector for channel 0 of the USB in the RZ/G1M Starter Kit Board is a mini connector shared by the USB host and function.

2.13.2. Block Diagram

![Block Diagram of USB2.0 Interface](image-url)

Figure 2.13.1 Block Diagram of USB2.0 Interface
2.14. Debug Serial Interfaces (SCIF0)

2.14.1. Specifications

On the RZ/G1M Starter Kit Board, the SCIF0 (port D) of the RZ/G1M are used as debug serial interface. The SCIF0 of the RZ/G1M is connected to the USB micro-AB connector (CN18) via the USB to UART bridge CP2102. By connecting CN18 to the host PC through a USB cable, this interface can be used as debug serial interface.

The SCIF0 has the features shown below. For details, see the SCIF specifications in the RZ/G Series User’s Manual: Hardware.

- Asynchronous serial communications
- Full-duplex communication supported
- Selectable bit rates by using the RZ/G1M’s on-chip baud-rate generator

The host PC connected to the RZ/G1M Starter Kit Board requires the CP2102 USB driver software. This driver software can be obtained from the following URL:
http://www.silabs.com/products/mcu/Pages/USBtoUARTBridgeVCPDrivers.aspx

Table 2.14.1 Debug Serial Interface Specifications

<table>
<thead>
<tr>
<th>Serial controller</th>
<th>RZ/G1M’s on-chip SCIF0 (port D)</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB to UART bridge</td>
<td>CP2102 (1 Mbps max.) by Silicon Laboratories</td>
</tr>
<tr>
<td>Connector</td>
<td>CN18: SCIF0, KS-MCR-B02T3-L by Weknowtechnology</td>
</tr>
</tbody>
</table>
2.15. Reset

2.15.1. Specifications

In the RZ/G1M Starter Kit Board specifications, the power-on reset signal is cleared by the reset IC MAX708SCSA, 200 ms after the 3.3-V power supply has settled. The power supplies for other voltage levels, 12.0 V, 5.0 V, 1.8 V, 1.5 V, and 1.0 V, are not monitored.

A power-on reset signal can be generated by pushing the push switch (SW9). The reset signal is level-shifted from 3.3 V to 1.8 V by the HD74ALVC1G07 and is input to the PRESET# pin of the RZ/G1M.

<table>
<thead>
<tr>
<th>Reset IC</th>
<th>MAX708SCSA by Maxim Integrated</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Threshold voltage: 2.93 V</td>
<td></td>
</tr>
<tr>
<td>• Reset delay time: 200 ms</td>
<td></td>
</tr>
</tbody>
</table>

2.15.2. Block Diagram

![Figure 2.15.1 Block Diagram of Reset Circuit](image-url)
2.16. I²C Interface

2.16.1. Specifications

The RZ/G1M incorporates seven I²C interface channels. Channels 5 and 6 are 1.8-V interfaces and channels 0 to 4 are 3.3-V interfaces. The following devices are connected to each channel of the I²C interfaces on the RZ/G1M Starter Kit Board.

<table>
<thead>
<tr>
<th>I²C controller</th>
<th>RZ/G1M’s on-chip I²C controller</th>
</tr>
</thead>
<tbody>
<tr>
<td>I²C devices through I²C (ch5)</td>
<td>[1.8 V]</td>
</tr>
<tr>
<td></td>
<td>CN23: External IO Connector</td>
</tr>
<tr>
<td>I²C devices through I²C (ch6)</td>
<td>[1.8 V]</td>
</tr>
<tr>
<td></td>
<td>U37: DA9063 by Dialog Semiconductor</td>
</tr>
<tr>
<td></td>
<td>U38: DA9210 by Dialog Semiconductor</td>
</tr>
<tr>
<td>I²C devices through I²C (ch4)</td>
<td>[3.3 V]</td>
</tr>
<tr>
<td></td>
<td>CN31: Touch screen connector</td>
</tr>
<tr>
<td>I²C devices through I²C (ch2)</td>
<td>[3.3 V]</td>
</tr>
<tr>
<td></td>
<td>U44: ADV7511WBSWZ by Analog Devices</td>
</tr>
<tr>
<td></td>
<td>U22: ADV7180WBCP32Z by Analog Devices</td>
</tr>
<tr>
<td></td>
<td>U24: AK4642EN by AKM Semiconductor</td>
</tr>
<tr>
<td></td>
<td>U50: R1EX24002ATAS0 by Renesas</td>
</tr>
<tr>
<td>I²C devices through I²C (ch1 port E)</td>
<td>[3.3 V]</td>
</tr>
<tr>
<td></td>
<td>U55: DA9063 by Dialog Semiconductor</td>
</tr>
</tbody>
</table>
2.17. External Interrupts

2.17.1. Specifications

The RZ/G1M has external interrupt input pins NMI, IRQ[9:0], INTC_IRQ[4:0]#, and INTC_EN[1:0]#. The RZ/G1M Starter Kit Board uses IRQ0, IRQ1, and IRQ2 as external interrupt input pins. It also uses GP3_29 and GP6_29 as GPIO interrupts. These pins should be used as active-low signals in programs. For the interrupt functions of the RZ/G1M, see the RZ/G Series User’s Manual: Hardware.

The devices and connectors of the interrupt request sources on the RZ/G1M Starter Kit Board are shown below.

<table>
<thead>
<tr>
<th>Interrupt Pin</th>
<th>Devices that Output Interrupt Request</th>
<th>Connectors</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRQ0</td>
<td>RMII PHY</td>
<td></td>
</tr>
<tr>
<td></td>
<td>U21: KSZ8041RNLI by Micrel</td>
<td></td>
</tr>
<tr>
<td>IRQ1</td>
<td>Touch Screen</td>
<td>CN31: GB10BXHAMLFSNP</td>
</tr>
<tr>
<td>IRQ2</td>
<td>PMIC</td>
<td></td>
</tr>
<tr>
<td></td>
<td>U55: DA9063 by Dialog Semiconductor</td>
<td></td>
</tr>
<tr>
<td>GP3_29</td>
<td>HDMI transmitter</td>
<td></td>
</tr>
<tr>
<td></td>
<td>U44: ADV7511WBSWZ by Analog Devices</td>
<td></td>
</tr>
<tr>
<td>GP6_29</td>
<td>Clock Synchronized Serial Device</td>
<td>CN6: 6-pin header</td>
</tr>
</tbody>
</table>

2.17.2. Block Diagram

A block diagram of external interrupts is shown below.

![Figure 2.17.1 Block Diagram of External Interrupts](image-url)
2.18. PWM

The RZ/G1M incorporates a seven-channel pulse width modulation timer (PWM). On the RZ/G1M Starter Kit Board, the use of other pin functions is given priority over the PWM functions in the case of pins that have multiplexed PWM functions. See the table below for details.

Table 2.18.1 Pin Functions Given Priority over PWM Functions

<table>
<thead>
<tr>
<th>PWM</th>
<th>Pin Functions Given Priority over PWM Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWM0</td>
<td>SD1_CD to SDHI1 interface</td>
</tr>
<tr>
<td>PWM0_B</td>
<td>GPIO (GP5_30)</td>
</tr>
<tr>
<td>PWM1</td>
<td>Mode pin 'MD8'</td>
</tr>
<tr>
<td>PWM1_B</td>
<td>SD1_WP to SDHI1 interface</td>
</tr>
<tr>
<td>PWM2W</td>
<td>LBSC 'BS#'</td>
</tr>
<tr>
<td>PWM2W_B</td>
<td>LBSC address 'A0'</td>
</tr>
<tr>
<td>PWM3</td>
<td>GPIO (GP1_24)</td>
</tr>
<tr>
<td>PWM4</td>
<td>GPIO (GP3_26)/DU1_DOTCLKOUT1</td>
</tr>
<tr>
<td>PWM4_B</td>
<td>Mode pin 'MD0'</td>
</tr>
<tr>
<td>PWM5</td>
<td>GPIO (GP7_21)</td>
</tr>
<tr>
<td>PWM5_B</td>
<td>GPIO (GP7_20)</td>
</tr>
<tr>
<td>PWM6</td>
<td>GPIO (GP7_22)</td>
</tr>
</tbody>
</table>
2.19. Clock

The RZ/G1M Starter Kit Board uses the crystal oscillators and resonators shown below.

2.19.1. Clocks Supplied to the RZ/G1M

<table>
<thead>
<tr>
<th>No.</th>
<th>Xn</th>
<th>Frequency</th>
<th>Pin Name on RZ/G1M</th>
<th>Type</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>X1</td>
<td>48.0000 MHz</td>
<td>USB_XTAL, USB_EXTAL</td>
<td>Resonator</td>
<td>-</td>
</tr>
<tr>
<td>2</td>
<td>X16</td>
<td>148.500 MHz</td>
<td>DU0_DOTCLKIN</td>
<td>Oscillator</td>
<td>1.8V</td>
</tr>
<tr>
<td>3</td>
<td>X3</td>
<td>20.0000 MHz</td>
<td>EXTAL</td>
<td>Oscillator</td>
<td>3.3V</td>
</tr>
</tbody>
</table>

2.19.2. Clocks Supplied to Devices Other than RZ/G1M

<table>
<thead>
<tr>
<th>No.</th>
<th>Xn</th>
<th>Frequency</th>
<th>Device</th>
<th>Device Pin Name</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>X9</td>
<td>25.0000 MHz</td>
<td>IDT5V41066</td>
<td>X1, X2</td>
<td>Resonator</td>
</tr>
<tr>
<td>2</td>
<td>X8</td>
<td>25.0000 MHz</td>
<td>KSZ8041RNLI</td>
<td>XI, XO</td>
<td>Resonator</td>
</tr>
<tr>
<td>3</td>
<td>X13</td>
<td>12.0000 MHz</td>
<td>ADV7511WBSWZ</td>
<td>CEC_CLK</td>
<td>Oscillator</td>
</tr>
<tr>
<td>4</td>
<td>X11</td>
<td>28.6363 MHz</td>
<td>ADV7180WBCP32Z</td>
<td>XTAL</td>
<td>Oscillator</td>
</tr>
<tr>
<td>5</td>
<td>X14</td>
<td>11.2896 MHz</td>
<td>AK4642</td>
<td>MCKI</td>
<td>Oscillator</td>
</tr>
<tr>
<td>6</td>
<td>X10</td>
<td>74.2500 MHz</td>
<td>SG-8002CE</td>
<td>CAN_CLK</td>
<td>Oscillator</td>
</tr>
<tr>
<td>7</td>
<td>X12</td>
<td>74.2500 MHz</td>
<td>SG-8002CE</td>
<td>IECLK_B</td>
<td>Oscillator</td>
</tr>
<tr>
<td>8</td>
<td>X15</td>
<td>74.2500 MHz</td>
<td>SG-8002CE</td>
<td>AVB_GTXREFCLK</td>
<td>Oscillator</td>
</tr>
</tbody>
</table>
2.20. Power Supply

2.20.1. Specifications

The RZ/G1M Starter Kit Board operates on a single 12.0-VDC power supply. The power supplies used for the RZ/G1M Starter Kit Board are generated by the switching regulators and low-dropout regulators. Specified sequences should be used to turn on and off the power supply to the RZ/G1M. Be sure to control the ACC switch (SW26) to obey the power sequence on the RZ/G1M Starter Kit Board.

See the table below for regulators used to generate power supplies on the RZ/G1M Starter Kit Board, their input voltage (Vin) and output voltage (Vout), and whether the ACC switch can be used to enable or disable output of power supplies.

### Table 2.20.1 List of RZ/G1M Starter Kit Board Switching Controllers and Regulators

<table>
<thead>
<tr>
<th>Vin</th>
<th>Vout</th>
<th>Switching Controller and Regulator</th>
<th>ACC Switch Control</th>
</tr>
</thead>
<tbody>
<tr>
<td>D12.0V</td>
<td>12.0V</td>
<td>-</td>
<td>Not supported</td>
</tr>
<tr>
<td>D5.0V / VSYS</td>
<td>IR 3838 (U576)</td>
<td>Supported</td>
<td></td>
</tr>
<tr>
<td></td>
<td>VTT</td>
<td>Dialog Semiconductor DA9063 (U55)</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>D1.8V</td>
<td>Dialog Semiconductor DA9063 (U55)</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>D1.0V</td>
<td>Dialog Semiconductor DA9063 (U55)</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>D1.35V</td>
<td>Dialog Semiconductor DA9063 (U55)</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>D3.3V</td>
<td>Dialog Semiconductor DA9063 (U55)</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>D1.8V_PERI</td>
<td>Dialog Semiconductor DA9063 (U55)</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>VCCQ1.8V</td>
<td>Dialog Semiconductor DA9063 (U55)</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>VLDO3_SD0 (3.3 / 1.8 V)</td>
<td>Dialog Semiconductor DA9063 (U55)</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>VLDO4_SD1 (3.3 / 1.8 V)</td>
<td>Dialog Semiconductor DA9063 (U55)</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>VI033 (3.3 V)</td>
<td>Dialog Semiconductor DA9063 (U55)</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>VLDO7_1.8V</td>
<td>Dialog Semiconductor DA9063 (U55)</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>VLDO8_SD2 (3.3 / 1.8 V)</td>
<td>Dialog Semiconductor DA9063 (U55)</td>
<td>Supported</td>
</tr>
<tr>
<td></td>
<td>DVFS1.0V</td>
<td>Dialog Semiconductor DA9210 (U56)</td>
<td>Supported</td>
</tr>
</tbody>
</table>

[Note]

As D12.0V is output to the following connectors, connecting or disconnecting an external board or a cable to these connectors must be performed while 12 V is not supplied to CN25 (while the 120-VAC switch is off).

- Power supply connector for serial-ATA interface (CN4)
- Connector for PCI Express (CN5)
- Back Light Header Connector (CN31)
2.20.2. Power-On Sequence

The diagram of the sequence for turning on the power (DA9063L-6B) for the RZ/G1M Starter Kit Board Rev2.0 is shown below.

*1 In the power-off sequence, turn off the power supplies in reverse order of the power-on sequence.

*2 The Co-PMIC (DA9210: DVFS1.0V and Core1.0V) are turned on/off with this ‘POWER_UP’ timing.

*3 ‘EXT_ON’ signal controls U581(MOS-SW: NX3P1108) to turn on/off D1.8V_Per(i ADV7511, ADV7180 etc)

*4 ‘ACC_CONT’ signal is used with other control signals to turn on/off 5V(VSYS).
   In the power-off sequence, ‘ACC_CONT’ keep 5V turn on.

*5 BUCKIO and BUCKMem are merge mode.

*6 BUCKCore1 and BUCKCore2 are merge mode.

*7 BUCKPeri provide D1.8V including VCC_ISO and D1.8V_Per

Figure 2.20.1 Power-On Sequence
3. **Outline Diagrams of RZ/G1M Starter Kit Board**

3.1. **External Dimensions and Hole Locations of RZ/G1M Starter Kit Board**

The following shows the external dimensions and hole locations of the RZ/G1M Starter Kit Board. (Unit: mm)

![Diagram](image)

**Figure 3.1.1 External Dimensions and Hole Locations of the RZ/G1M Starter Kit Board**

*(Top View)*
3.2. Connector Locations on RZ/G1M Starter Kit Board (Component Surface)

The following shows the connector locations on the component surface.

Figure 3.2.1 Connector Locations of the RZ/G1M Starter Kit Board (Component Surface) (Top View)
3.3. **Connector Locations on RZ/G1M Starter Kit Board (Solder Surface)**

The following shows the connector locations on the solder surface.

![Connector Locations on RZ/G1M Starter Kit Board (Solder Surface)](image)

*Figure 3.3.1 Connector Locations of the RZ/G1M Starter Kit Board (Solder Surface) (Bottom View)*